	Type	L #	Hits	Search Text	DBs	Time Stamp
1	IS&R	L1	2	(("6245580") or ("5851841")).PN.	USPAT	2001/08/14 13:46
2	BRS	L2	0	(columnar with microstructure with ferroelectric) and @ad<19991029	USPAT; US-PGPUB	2001/08/14 13:54
3	BRS	L3	0	((columnar with microstructure) same ferroelectric) and @ad<19991029	USPAT; US-PGPUB	2001/08/14 13:55
4	BRS	L4	0	((column with microstructure) same ferroelectric) and @ad<19991029	USPAT; US-PGPUB	2001/08/14 13:55
5	BRS	L5	0	((column same microstructure) same ferroelectric) and @ad<19991029	USPAT; US-PGPUB	2001/08/14 13:55
6	BRS	L6	55	(microstructure same ferroelectric) and @ad<19991029	USPAT; US-PGPUB	2001/08/14 15:40
7	BRS	L7	2	6 and columnar	USPAT; US-PGPUB	2001/08/14 14:29
8	BRS	L8	6	6 and (lower adj electrode)	USPAT; US-PGPUB	2001/08/14 14:29
9	BRS	L9	1	8 and columnar	USPAT; US-PGPUB	2001/08/14 14:30
10	BRS	L10	10	(microstructure same ferroelectric) and @ad<19991029	EPO; JPO; DERWENT	2001/08/14 15:35
11	BRS	L11	0	10 and columnar	EPO; JPO; DERWENT	2001/08/14 15:35
12	BRS	L12	55	(microstructure same ferroelectric) and @ad<19991029	USPAT; US-PGPUB	2001/08/14 15:43
13	BRS	L13	2	12 and columnar	USPAT; US-PGPUB	2001/08/14 15:41

enough

	Type	L #	Hits	Search Text	DBs	Time Stamp
14	BRS	L14	251	microstructure and ferroelectric and @ad<19991029	USPAT; US-PGPUB	2001/08/14 15:43
15	BRS	L15	14	14 and columnar	USPAT; US-PGPUB	2001/08/14 15:43

	Comments	Error Definition	Errors
14			0
15			0

DOCUMENT-IDENTIFIER: US 6190728 B1
TITLE: Process for forming thin films of functional ceramics

APD:
19980928

DEPR:
The electrical properties of a **ferroelectric** thin film with a perovskite structure largely depend on the **microstructure** and orientation of the resultant film. Highly oriented film of a perovskite structure shows excellent electrical properties. In the above description, the PZT layers in the multi-layered PZT-PT film annealed at 500.degree. C. are supposed to have higher relative permittivity. Therefore, the microstructures of the resultant thin films prepared by the different processes and/or annealed at different temperatures were observed by the FE-SEM. The results are shown in FIGS. 6 and 7.

DEPR:
On the other hand, the films annealed at 500.degree. C. show quite different microstructures as seen in FIGS. 7A and 7B. The PZT film prepared by the single-seeding process shows almost the same microstructure as that of the films annealed at 450.degree. C. except the grain size, while the PZT film prepared by the multi-seeding process has a **columnar**-like structure. This **columnar**-like structure is attributed to the stacking structure of the film obtained by the multi-seeding process. However, it is very difficult to recognize the formation mechanism of the **columnar** structure and a further investigation is required to know it.

DEPR:
The first coating of the PT seeding layer can be a buffer layer to protect the

interaction between the electrode and the film. In addition, this structure
shows that a reaction occurs between the PT film and the PZT film forming the
solid solution by annealing at 500.degree. C. Therefore, the resultant
multi-layered thin film has a composition rich in titanium. In spite of such
titanium rich composition, the resultant film shows better dielectric property
than the film prepared by the single-seeding process because of their **columnar**
microstructure.

DOCUMENT-IDENTIFIER: US 5986724 A
TITLE: Liquid crystal display with liquid crystal layer and ferroelectric layer
connected to drain of TFT

APD:
19970227

DRPR:
FIG. 40 a schematic diagram showing the **microstructure of a ferroelectric** thin
film formed by heteroepitaxial growing;

DEPR:
In FIG. 23, reference numeral 501 denotes a scan line, 502 a data line, 503 a
gate electrode, 504 a drain electrode, 505 a **lower electrode,** 506 a
ferroelectric layer, and 507 a pixel electrode.

DEPR:
On the other hand, after depositing the gate insulator film, a **lower electrode**
608 with ferroelectric capacitance was formed, a ferroelectric layer 611 was
deposited thereon, and patterning was performed. As the ferroelectric
substance, the above-described various materials may be used.

DEPR:
Then, an electrode on the ferroelectric substance and a pixel electrode 612
were formed. And, the **lower electrode** 608 and the drain electrode 610 were
contacted to electrically connect mutually.

DEPR:
Lastly, an insulator film 615 was deposited on the whole surface and removed
from the pixel portion. The insulator film 615 can be a silicon nitride film,
a light-absorbing organic insulator film (such as a pigment dispersion type
acrylic resin), or the like. For the **lower electrode** 608 and the upper
electrode 612, an indium-tin oxide film ITO was used. Thus, the

ferroelectric
substance allows the passage of light, and a transmission type display mode can
be used. But, the electrode material may be platinum, gold or other materials.
It is also possible that the electrodes are multilayered, the ferroelectric
substance side is ITO, and the other side is molybdenum or aluminum. A liquid
crystal 613, an opposed electrode 614a and an opposed substrate 614 may have
the same structure as the one shown in FIG. 22.

DEPR:
The device shown in this drawing has a scan line 904 for selecting a transistor
901 and a data line 905 for supplying a signal; and it is characterized to
apply a potential to an electrode 907 within an element 902 containing a
ferroelectric substance in order to apply a voltage to a liquid crystal 903.
The element 902 has the ferroelectric substance between a **lower electrode** 909
and the electrode 907 to control a polarization of the ferroelectric substance
with a voltage applied to the electrode 907, and an electric field produced by
the electric charge generated around the electrode 907 is applied to the liquid
crystal.

DEPR:
Furthermore, the **lower electrode,** the second electrode 1001, is not restricted
to the one which is fully faced with the first electrode 1003 as shown in FIG.
28. The second electrode can also be patterned in the form of a mesh and can
be used to control the lines of electric force formed between the first
electrode 1003 and the second electrode 1001. For example, the lines of
electric force in a slant direction are positively used to control a
polarization vector, and a vertical component strength can be changed spatially
by the applied voltage. In this case, the insulator film 1004 may be either a
ferroelectric substance or not. Thus, an area gradational effect

can be given.

DEPR:
In the drawing, reference numeral 1101 denotes an insulating substrate. The insulating substrate 1101 has a transistor 1103 and an element 1102 containing a ferroelectric substance. Reference numeral 1111 is an opposed substrate which has an opposed electrode 1110. A liquid crystal 1109 is intervened between the insulating substrate 1101 and the opposed substrate 1111. The transistor 1103 comprises a semiconductor layer 1114, source and drain electrodes 1112, 1113, a gate insulator film 1115, and a gate electrode 1116. The element 1102 including the ferroelectric substance has a **lower electrode** 1104, a ferroelectric layer 1105, and an upper electrode 1106. Reference numeral 1107 denotes an insulator film, and 1108 a pixel electrode.

DEPR:
FIG. 31 is a modification from the one shown in FIG. 27. The apparatus shown in FIG. 31 has a scan line 1404 for selecting a transistor 1401, and a data line 1405 for supplying a signal; to apply a voltage to a liquid crystal 1403, a potential is applied to an electrode 1407 within an element 1402 containing a ferroelectric substance. The element 1402 has the ferroelectric substance between a **lower electrode** 1409 and the electrode 1407. And, differences from the one shown in FIG. 27 are that a drain of the transistor 1401 is connected to the **lower electrode** 1409, and the electrode 1407 is connected to its neighboring scan line 1408.

DEPR:
And, the ferroelectric capacitance in the structure shown in FIG. 26 may be replaced with the element 902 or 1402 which has the ferroelectric element intervened between the **lower electrode** and the electrode shown in FIG. 27 or

FIG. 31. Such a structure is shown in FIG. 34 and FIG. 35.

DEPR:
To form the film, a CVD method which is one of vapor phase epitaxy was used in this embodiment. FIG. 40 shows a microstructure of the pixel section. The microstructure was an aggregate of **columnar** grains, which is called a **columnar** structure. And, it was found to be in a highly oriented state (generally called as epitaxial growth in a broad sense) with reference to an X-ray diffraction pattern. It is considered to owe to the matching of the lattice constant and thermal expansion with the pixel electrode material.

DEPR:
Such a structure indicates that most of the **columnar** grains can be grown in the same axial direction with respect to the vertical direction of the substrate.

DEPR:
When the surface area of each of the **columnar** grains is large enough for the liquid crystal to make an optical response, the **columnar** grains can be regarded as domains.

DEPR:
In this embodiment, it is designed that the voltage applied to the respective **columnar** grains does not vary. Thus, the plane division in the pixel region can be achieved.

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	0	((Ar with O2) with annealing) and ferroelectric	USPAT	2001/08/14 10:28
2	BRS	L2	0	((Ar with O2) with annealing) and ferroelectric	USPAT; US-PGPUB	2001/08/14 10:32
3	BRS	L3	0	((N2 with O2) with annealing) and ferroelectric	USPAT; US-PGPUB	2001/08/14 10:33
4	BRS	L4	0	((Ar with N2O) with annealing) and ferroelectric	USPAT; US-PGPUB	2001/08/14 10:33
5	BRS	L5	1	((Ar with NO) with annealing) and ferroelectric	USPAT; US-PGPUB	2001/08/14 11:28
6	BRS	L6	0	((Ar with NO2) with annealing) and ferroelectric	USPAT; US-PGPUB	2001/08/14 10:34
7	BRS	L7	115	(ferroelectric same crystallization) and annealing	USPAT; US-PGPUB	2001/08/14 11:29
8	BRS	L8	5	7 and (annealing with air) and @ad<19991029	USPAT; US-PGPUB	2001/08/14 11:30

— enough —

DOCUMENT-IDENTIFIER: US 6245580 B1
TITLE: Low temperature process for fabricating layered superlattice materials
and making electronic devices including same

APD:
19990111

BSPR:
Integrated circuit devices containing **ferroelectric** elements with layered
superlattice materials are currently being manufactured. The layered
superlattice materials comprise metal oxides. The presence of oxides causes
problems because the oxygen diffuses through the various materials contained in
the integrated circuit and combines with atoms in the substrate and in
semiconductor layers forming oxides. The resulting oxides interfere with the
function of the integrated circuit; for example, they may act as dielectrics in
the semiconducting regions, there by virtually forming capacitors. Diffusion
of atoms from the underlying substrate and other circuit layers into the
ferroelectric metal oxide is also a problem; for example, silicon from a
silicon substrate and from polycrystalline silicon contact layers is known to
diffuse into layered superlattice material and degrade its **ferroelectric**
properties. For relatively low-density applications, the **ferroelectric** memory
capacitor is placed on the side of the underlying CMOS circuit, and this may
reduce somewhat the problem of undesirable diffusion of atoms between circuit
elements. Nevertheless, as the market demand and the technological ability to
manufacture high-density circuits increase, the distance between circuit
elements decreases, and the problem of molecular and atomic diffusion between
elements becomes more acute. To achieve high circuit density by reducing

circuit area, the **ferroelectric** capacitor of a memory cell is placed virtually on top of the switch element, typically a field-effect transistor (hereinafter "FET"), and the switch and bottom electrode of the capacitor are electrically connected by a conductive plug. To inhibit undesired diffusion, a barrier layer is located under the **ferroelectric** oxide, between the capacitor's bottom electrode and the underlying layers. The barrier layer not only must inhibit the diffusion of oxygen and other chemical species that may cause problems; it must also be electrically conductive, to enable electrical connection between the capacitor and the switch. The maximum processing temperature allowable with current barrier technology is about 700.degree. C. At temperatures above 700.degree. C., the highest-temperature barrier materials degrade and lose their diffusion-barrier properties. On the other hand, the minimum feasible manufacturing process temperatures of layered superlattice materials used in the prior art is about 800.degree. C., which is the temperature at which deposited layered superlattice materials are annealed to achieve good **crystallization**. Good **ferroelectric** properties have been achieved in the prior art using process heating temperatures at about 700.degree. C. See U.S. Pat. No. 5,508,226, issued Apr. 16, 1996, to Ito et. al. Nevertheless, the **annealing** and other heating times in the low-temperature methods disclosed in the prior art are in the range of three to six hours, which is economically unfeasible.

BSPR:
An important feature of the invention is that heating comprises a step of **annealing** the coating at a temperature not exceeding 700.degree. C., preferably for a time period not exceeding one and one-half hours. In one embodiment of the invention, the **annealing** is conducted in an

oxygen-enriched
ambient, typically in O.sub.2 gas. In another embodiment of the invention, the
annealing is conducted in oxygen-deficient ambient, typically substantially
pure nitrogen gas (hereinafter "N.sub.2 gas").

BSPR:
In one aspect of the invention, the substrate comprises a first electrode, and
the method includes steps of forming a second electrode on the coating, after
the step of **annealing**, to form a capacitor, and subsequently performing a step
of post-**annealing**. In a preferred embodiment, the first electrode and the
second electrode contain platinum and titanium. The step of post-**annealing** is
conducted at a temperature not exceeding 700.degree. C., preferably for a time
period not exceeding 30 minutes. In one embodiment of the invention, the
post-**annealing** is conducted in an oxygen-enriched ambient, typically in O.sub.2
gas. In another embodiment of the invention, the post-**annealing** is conducted
in oxygen-deficient ambient, typically N.sub.2 gas.

BSPR:
In a preferred embodiment of the inventive method, the heating comprises steps
of baking the coating, rapid thermal processing the coating, **annealing** the
coating, and post-**annealing** the coating. It is a feature of the invention that
the total amount of time during which all of these heating steps are conducted
does not exceed two hours.

DEPR:
In **annealing** step 230, the coating is annealed at a temperature not exceeding
700.degree. C. to form the thin film of layered superlattice material. The
annealing time does not exceed one and one-half hours. Preferably, the
annealing time is about 60 minutes. The anneal is typically performed in a
furnace containing an O.sub.2 gas ambient, but good experimental

results were
also obtained using an oxygen-free N.sub.2 gas ambient. The **annealing** step can
also be conducted in **air**, in an oxygen-enriched ambient, or in an "oxygen-deficient" ambient in which the relative amount of oxygen is less than
the relative amount of oxygen in **air**. The sequence of steps 224-230 may be
conducted a second time (indicated by the dashed flowline in FIG. 2) to achieve
the desired quality and thickness of the ferroelectric thin film. Depending on
the thickness of the initial coating, the thickness of the thin film after one
sequence of steps 224-230 ranges between 40 nm and 100 nm. Preferably, two
sequences of steps 224-230, each sequence forming a layer with a thickness of
40-50 nm, are used to form a ferroelectric thin film with a total thickness of
80-100 nm. For process-economical reasons, however, it might be desirable to
form a thin film of 80-100 nm thickness using one sequence of steps 224-230.
Or, for example, to increase circuit density, it might be preferable to use one
sequence of steps 224-230 to form a thin film having a thickness in the range
of 40-50 nm.

DEPR:
In step 234, post-**annealing** is performed at a temperature not exceeding
700.degree. C. Preferably, post-**annealing** step 234 is performed for a time
period not exceeding 30 minutes. Post-**annealing** step 234 may be performed in
substantially pure O.sub.2 gas or in substantially pure N.sub.2 gas or in
mixtures of the two gases, such as **air**. As deposited, the adhesion of the top
electrode to the thin film of layered superlattice material is usually weak.
The adhesion is improved by post-**annealing**. The post-anneal is preferably
performed in an electric furnace at a temperature between 500.degree. C. and
the anneal temperature, which does not exceed 700.degree. C. A post-anneal

below 500.degree. C. does not improve the adhesion of the electrode, and the
resulting capacitor devices would tend to be extremely leaky, and shorted in
the worst cases.

DEPR:
The post-anneal releases the internal stress in the top electrode and in the
interface between the electrode and the ferroelectric thin film. At the same
time, the post-**annealing** step 234 reconstructs microstructure in the layered
superlattice material resulting from the sputtering of the top electrode, and
as a result improves the properties of the material. The effect is the same
whether the post-anneal is performed before or after the patterning steps
mentioned in connection with step 236 below. The effect of oxygen ambient
during the post-anneal is not as clear as it is in RTP step 228 and anneal step
230 because the layered superlattice material is covered by the top electrode
and not exposed to the ambient atmosphere. With regard to most electrical
properties, inert gas, such as helium, argon, and nitrogen, may be used with
approximately the same result as with oxygen. Nevertheless, it has been found
that an oxygen ambient during the post-anneal improves the crystallographic
order at the interface of the top electrode and the ferroelectric thin film, as
well as the symmetry of the hysteresis curve.

DEPR:
Strontium bismuth tantalate capacitors were prepared as in Example 1, also
using only one spin-coating of precursor and, therefore, only one sequence of
spin-coating, baking, RTP and **annealing** steps. But, in this second example,
the final ferroelectric thin film had a measured thickness of only 47.5 nm.
Also, the hot-plate bake was performed at 160.degree. C. for one minute, as in
Example 1, but then at 260.degree. C. for only two minutes, instead of four

minutes. Measurements were performed similar to those conducted with the
capacitors of Example 1.

DEPR:
Strontium bismuth tantalate capacitors were prepared as in Example 2, except
that two spin-coatings were used to form the thin film of layered superlattice
material. The sequence of spin-coating, baking, RTP and **annealing** steps was
conducted two times, each sequence depositing a film about 40 nm thick. The
final ferroelectric thin film had a thickness of about 85 nm, comparable to the
thickness of the thin film in Example 1. In contrast to Examples 1 and 2, the
annealing step and the post-**annealing** step were conducted in N.sub.2 gas
(instead Of O.sub.2 gas). Measurements were performed similar to those
conducted with the capacitors of Example 1.

CLPR:
9. A method as in claim 1, wherein said heating comprises a step of **annealing**
said coating at a temperature not exceeding 700.degree. C.

CLPR:
10. A method as in claim 9, wherein said step of **annealing** is conducted for a
time period not exceeding one and one-half hours.

CLPR:
11. A method as in claim 9, wherein said step of **annealing** is conducted in an
oxygen-enriched ambient.

CLPR:
12. A method as in claim 9, wherein said step of **annealing** is conducted in an
oxygen-deficient ambient comprising nitrogen.

CLPR:
13. A method as in claim 12, wherein said step of **annealing** is conducted in
substantially pure N.sub.2 gas.

CLPR:

14. A method as in claim 1, wherein said substrate comprises a first
electrode, and further comprising steps of forming a second electrode on said
coating, after said step of heating, to form a capacitor, and subsequently
performing a step of post-**annealing**.

CLPR:
16. A method as in claim 14, wherein said step of post-**annealing** is conducted
at a temperature not exceeding 700.degree. C. for a time period not exceeding
30 minutes.

CLPR:
17. A method as in claim 16, wherein said step of post-**annealing** is conducted
in an oxygen-enriched ambient.

CLPR:
18. A method as in claim 17, wherein said step of post-**annealing** is conducted
in an oxygen-deficient ambient comprising nitrogen.

CLPR:
19. A method as in claim 18, wherein said step of post-**annealing** is conducted
in substantially pure N.sub.2 gas.

CLPR:
21. A method as in claim 1, wherein said heating comprises steps of baking
said coating, rapid thermal processing said coating, **annealing** said coating,
and post-**annealing** said coating.

DOCUMENT-IDENTIFIER: US 6172385 B1
TITLE: Multilayer ferroelectric capacitor structure

APD:
19981030

BSPR:
Layered **ferroelectric** films such as strontium bismuth tantalate (SBT),
strontium bismuth niobate (SBN) and strontium bismuth tantalate niobate (SBTN)
generally require long **annealing** times (on the order of 30-90 minutes or
longer) and high processing temperatures (800.degree. C.) for optimum film
crystallization and electrical properties. The resultant **ferroelectric** films
are characterized as having highly asymmetric grains and an inherent porosity.

BSPR:
If lower processing temperatures or times are employed, the resultant
ferroelectric films typically exhibit poor leakage behavior, low remanent
polarization and low fatigue. In addition, under prior art **annealing**
conditions, oxidation of the electrodes and the underlying contacts may result
in high resistivity contacts.

BSPR:
Moreover, by utilizing prior art **annealing** conditions, interfacial layers may
result between the electrodes and underlying contact and/or between the
ferroelectric material and the electrode. For instance, Bi readily forms Bi/Pt
alloys which may degrade the performance of the capacitor.

BSPV:
(b) **annealing** said multilayer ferroelectric film at a temperature below
800.degree. C. for a time period of from about 5 to about 120 minutes.

DEPR:
After depositing the multilayer ferroelectric film, the ferroelectric film is annealed using conditions which have not yet been used in processing such films. As stated in the background section of this application, single layer ferroelectric films are typically processed, i.e. annealed, at temperatures at or about 800.degree. C. for time periods of from about 30 minutes or higher. In accordance with the method of the present invention, the deposited multilayer ferroelectric film is annealed using a low temperature, rapid anneal process. Specifically, **annealing** is carried out in an oxidizing gas such as oxygen, N.sub.2 O, ozone or mixtures of gases including an oxidizing gas, e.g. **air,** at temperatures below 800.degree. C. for a time period of from about 5 to about 120 min. Preferred **annealing** conditions are at a temperature of from about 500.degree. to about 750.degree. C. for a time period of from about 10 to about 60 min.

DOCUMENT-IDENTIFIER: US 5998819 A
TITLE: Thin ferroelectric film element having a multi-layered thin
ferroelectric film and method for manufacturing the same

APD:
19980812

BSPR:
(2) Step of annealing and drying the obtained film at 150.degree. C. for 30
seconds to several minutes for removing, from the film, the solvent and the
alcohol and residual water that have been generated by the reaction of step
(1);

BSPR:
(3) Step of annealing the film at 725.degree. C. for 30 seconds under oxygen
atmosphere by employing a RTA (Rapid Thermal Annealing) method for removing the
organic components in the film by thermal decomposition; and

BSPR:
(4) Step of annealing the film at 800.degree. C. for one hour under oxygen
atmosphere for crystallization of the film;

BSPR:
(5) Step of annealing the film at 800.degree. C. for 30 minutes under oxygen
atmosphere after an upper electrode is formed.

BSPR:
However, by a method of manufacturing a thin ferroelectric film using the
above-mentioned conventional MOD method, little crystallization of the thin
ferroelectric film takes place at annealing temperature of 650.degree. C. or
less. Accordingly, in order to obtain a high residual polarization, it is
necessary to carry out an annealing step at an extremely high temperature of
800.degree. C. for a period of time as long as one hour (International

Application No. PCT/US93/10021). Therefore, in forming a thin ferroelectric film element on an integrated circuit having a stack structure, there will occur damages such as poor contact and deterioration in characteristics due to interdiffusion and oxidation between the viahole (contact hole) material and the electrode material, thus placing a hindrance particularly in manufacturing such highly integrated devices.

BSPR:
Also, since the annealing temperature is thus high, the particle diameter of the crystal particles constituting the thin ferroelectric film is as large as 1000 to 2000 .ANG. and the irregularity on the surface of the thin film is large. Accordingly, it has not been possible to apply the conventional MOD method to fine submicron processing which is required in manufacturing highly integrated devices.

BSPR:
Moreover, in the case of highly integrated FRAMs of 4M bit to 16M bit or more, the capacitor area will be small and the spontaneous residual polarization Pr required in the ferroelectric materials will be large, so that Pr of at least 10 .mu.C/cm.sup.2 will be necessary. In the case of the thin SrBi.sub.2 Ta.sub.2 O.sub.9 film, the spontaneous residual polarization Pr will be small in accordance with the decrease in the annealing temperature, so that it has not been possible to obtain sufficient Pr required in highly integrated FRAMs by conventional methods if the annealing temperature is lowered.

BSPR:
The present invention also provides a method of manufacturing the above-mentioned thin ferroelectric film element comprising: forming the lower thin electrode film on the substrate; applying each of a plurality of precursor solutions containing partially different metal elements and drying to form a

laminate film of at least three layers comprising at least two kinds of films;
performing a first annealing; forming the upper thin electrode film; and
performing a second annealing.

BSPR:
Thus, the present invention provides a thin ferroelectric film element in which
a sufficiently high spontaneous residual polarization and a sufficiently low
coercive field are achieved at an annealing temperature lower than that by
conventional methods, the thin ferroelectric film element being applicable to
highly integrated FRAMs.

DEPR:
The thin ferroelectric film according to the present invention may be formed by
a physical method such as vacuum vapor deposition method, sputtering method and
laser abrasion method, or by a chemical method such as sol-gel method, MOD
method and MOCVD method using an organic metal compound as a starting material.
Among these, a preferable method is a sol-gel method involving a series of
steps including applying each of a plurality of precursor solutions containing
partially different metal elements and drying to form a thin ferroelectric film
of at least three layers comprising at least two kinds of thin ferroelectric
films, performing a first annealing step, forming an upper thin electrode film,
and performing a second annealing step.

DEPR:
Subsequently, a first annealing step is preferably performed after the thin
ferroelectric film has been formed. The first annealing step is preferably
carried out under an oxygen atmosphere or in an air at a temperature of about
500 to about 600.degree. C. for about 1 to 60 minutes. The first annealing
step may be carried out by employing a conventional method such as RTA method
or heat treatment using a thermal processing furnace.

DEPR:
Then, the upper thin electrode film is formed. The upper thin electrode film may be formed of the above-mentioned electrically conductive material by employing a conventional method such as vacuum vapor deposition method, sputtering method, EB vapor deposition method or the like. A second annealing step is preferably performed after the upper thin electrode film has been formed. The second annealing step is preferably carried out under an oxygen atmosphere or in an air at a temperature of about 600 to 800.degree. C. for about 1 to 60 minutes. The second annealing step may be carried out by employing a conventional method such as RTA method or heat treatment using a thermal processing furnace. By these annealing steps, it is possible to form a thin ferroelectric film which is dense and has good surface flatness.

DEPR:
A provisional annealing was then conducted in an oxygen atmosphere at 580.degree. C. for 30 minutes as the first annealing by employing RTA (Rapid Thermal Annealing) method (step S29), and an upper Pt electrode 6 was deposited to a thickness of 150 nm using a mask by EB (Electron Beam) deposition method to form an electrode of 100 .mu.m .O slashed. (step S30).

DEPR:
A main annealing was then conducted in an oxygen atmosphere at 750.degree. C. for 30 minutes as the second annealing by employing RTA method (step S31).

DEPR:
Specifically, the precursor solution for the first SBT layer was first applied on the substrate at 5000 rpm for 20 seconds by spin coating method, and the substrate was baked in an oven at 115.degree. C. for 15 minutes in a drying step. A provisional annealing step was then conducted at

400.degree. C. for
60 minutes. The second BTO layer and the third SBT layer were formed in the
same manner as in the above process. Subsequently, a main annealing step was
conducted in an oxygen atmosphere at 650.degree. C. for 15 seconds by RTA
method to form the laminated thin ferroelectric film of SBT layer/BTO layer/SBT
layer. An upper electrode was formed on the laminated thin ferroelectric film
thus formed in the same manner as in the above Example 1 to complete the thin
ferroelectric film element according to this Example.

DEPR:
According to the thin ferroelectric film element of the present invention thus
described, it is possible to manufacture an element which can achieve
sufficiently high spontaneous residual polarization and sufficiently low
coercive field with a lower annealing temperature than by the conventional
methods and in which the operating voltage is small, the leakage current is
small, and the fatigue characteristics are excellent.

CLPV:
performing a first annealing;

CLPV:
performing a second annealing.

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	115	(ferroelectric same crystallization) and annealing	USPAT; US-PGPUB	2001/08/14 09:15
2	BRS	L2	31	1 and (Ar or N2 or He or Ne or Xe) and (O2 or N2O or No or No2)	USPAT; US-PGPUB	2001/08/14 08:25
3	BRS	L3	31	1 and (Ar or N2 or He or Ne or Xe) and (O2 or N2O or NO or NO2)	USPAT; US-PGPUB	2001/08/14 08:25
4	BRS	L4	30	3 and @ad<=19991029	USPAT; US-PGPUB	2001/08/14 08:25
5	BRS	L5	8	(ferroelectric same crystallization) and annealing	EPO; JPO; DERWENT	2001/08/14 09:16
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1 **Dielectric properties of sol-gel derived barium-strontium-titanate (0.4/Sr/sub 0.6/TiO/sub 3/) thin films**
Lahiry, S.; Gupta, V.; Sreenivas, K.; Mansingh, A.
Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions on , Vo
Issue: 4 , July 2000
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2 **Orientation of PZT thin films prepared by sol-gel techniques**
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3 **Preparation and ferroelectric properties of graded Pb(Ti/sub x/Zr, 1-x/)O/sub 3/ thin films**
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4 **The structure and degradation mechanism of ferroelectric SrBi/sul 2/Ta/sub 2/O/sub 9/ thin films**
Hong Keun Kim; Song Hun Kim; Sang Bo Bae; Ill Won Kim; Pichugin, V.F.; T.S.; Stoliarenko, V.F.
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8 **RF sputtered PLZT thin film on Pt/Ti electrode**
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9 **Properties of sol-gel-derived lead zirconate titanate (PZT) thin filn platinum-coated silicon substrates**
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10 **PZT thin film preparation on Pt/Ti electrode by RF magnetron spu**
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13 **The effect of annealing temperature on the formation of SrBi/sub 2/Ta/sub 2/O/sub 9/ (SBT) thin films**
Ravichandran, D.; Yamakawa, K.; Roy, R.; Bhalla, A.S.; Trolier-McKinstry, S Cross, L.E.
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14 **Microstructure development in lead zirconate titanate ferroelectri films during annealing**
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15 **A novel process for alkoxide-derived PZT thin films with multi-see layers**

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1 2 [Next]

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ferroelectric <and> crystallization <and> annealing

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16 **Study on preparation of Pb(Zr,Ti)O/sub 3/ thin-films on TiNi SMA substrates using sol-gel techniques**
Xinshan Li; Jinrong Cheng; Qingfeng Liu; Jiancheng Zhang; Zhongyan Meng
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18 **The formation of a fine-patterned ferroelectric thin film from a so solution containing a photo-sensitive water-generator**
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DOCUMENT-IDENTIFIER: US 5851841 A
TITLE: Method for producing ferroelectric film element, and ferroelectric film
element and ferroelectric memory element produced by the method

APD:
19960913

BSPR:
As ferroelectric materials for these applications, oxide materials of
perovskite structure represented by PZT (lead zirconium titanate, Pb (Ti, Zr)
O.sub.3) are mainly used. However, there is a problem with materials
containing lead as their component element such as PZT, that the lead is
evaporated when forming the film because of high evaporation pressure of lead
or its oxide, so that defects take place in the film or in the worst case
pinholes are formed. Consequently, they had a fault that the leakage current
increased and further repetition of polarization reversals led to fatigue
phenomena such a decrease in the magnitude of spontaneous polarization. In
particular, if a substitution of ferroelectric nonvolatile memories for FRAM is
considered, **no** change in characteristics even after 10.sup.15 times of
polarization reversals must be ensured concerning fatigue phenomena and
therefore development of ferroelectric films free from fatigue has been
desired.

BSPR:
In this conjunction, research and development of bismuth layer-structured
composition materials has recently been carried out. Bismuth layer-structured
composition materials were discovered in 1959 by Smolenskii and others (G. A.
Smolenskii, V. A. Isupov and A. I. Agranovskaya, Soviet Phys. Solid State, 1,
149, (1959)) and thereafter were examined in detail by Subbarao

(E. C.
Subbarao, J. Phys,. Chem. Solids, 23, 665 (1962)). Lately, Carlos A. Paz de
Araujo and others found out that this bismuth layer-structured composition is
suitable for the application to ferroelectric and high-dielectric integrated
circuits and reported a superior fatigue property that **no** change in
characteristics were observed in particular even after 10.sup.12 times or more
of polarization reversals (International Application **No.** PCT/US92/10542).

BSPR:
In particular, as film forming method of the above bismuth layer-structured
film, the MOD method is employed. With a film forming process in accordance
with the conventional MOD method, ferroelectric films or dielectric films are
produced in the following steps (International Application **No.** PCT/US92/10542,
PCT/US93/10021).

BSPR:
In the above-mentioned method for producing a **ferroelectric** film by using a
conventional MOD method, however, **ferroelectric** films obtained by the step of
crystallization prior to the formation of the upper electrode (step 4) are
hardly crystallized at **annealing** temperatures of 650.degree. C. or lower and
had to be treated by heating at an extreme high temperature of 800.degree. C.
for as long a time as an hour to obtain a high remanent polarized value
(International Application **No.** PCT/US93/10021). Accordingly, the obtained film
became a coarse-structured film with the grain size on the order of about 2000
.ANG. and the insulating resistance decreased with increasing leakage current,
thereby making the fine machining more difficult, and therefore the
conventional MOD method was not fit for the highly integration.

BSPR:

As mentioned above, in the method for producing a **ferroelectric** film element employing the sol-gel method and the MOD method according to the present invention, after applying a precursor solution comprising component elements of a **ferroelectric** film material to the substrate and drying, the conventional RTA heat treatment step for removing the organic component in the film is omitted and the application drying step is repeated at several times to form a predetermined film thickness, then organic substances are removed by pyrolysis in a first heat treatment step and at the same time **crystallization** is carried out. And as a second heat treatment step after the formation of an upper electrode layer on this heat-treated film, the **ferroelectric** film is crystallized by drying for a sufficient time in the atmosphere of gas pressure at 1 atm or lower.

BSPV:
3) The process of heat treatment at 725.degree. C. for 30 sec. by using the RTA (Rapid Thermal **Annealing**) method in the oxygen atmosphere to remove the organic components in the film by pyrolysis.

DRPR:
FIG. 3 is a graph showing a change in remanent polarization relative to a second **annealing** temperature of the first embodiment;

DRPR:
FIG. 4 is a graph showing a change in coercive field Ec relative to a second **annealing** temperature of the first embodiment;

DRPR:
FIG. 5 is a graph showing a change in accumulated charge .delta.Q relative to a second **annealing** temperature of the first embodiment;

DRPR:
FIG. 10 is a graph showing a change in leakage current density under

application of 3 V relative to a second **annealing** temperature of the first
embodiment;

DRPR:
FIG. 11 is a SEM photograph of the surface of a film produced with a first
annealing temperature set at 600.degree. C. and a second **annealing** temperature
set at 600.degree. C. in the producing method of FIG. 2;

DRPR:
FIG. 13 is a graph showing a change in remanent polarization Pr relative to a
second **annealing** temperature of a conventional ferroelectric element;

DRPR:
FIG. 14 is a graph showing a change in coercive field Ec relative to a second
annealing temperature of a conventional ferroelectric element;

DRPR:
FIG. 15 is a graph showing a change in accumulated charge .delta.Q relative to
a second **annealing** temperature of a conventional ferroelectric element;

DRPR:
FIG. 16 is a graph showing a change in leakage current density under
application of 3 V relative to a second **annealing** temperature of a conventional
ferroelectric element;

DRPR:
FIG. 17 is a SEM photograph of the surface of a film produced with a first
annealing temperature set at 600.degree. C. and a second **annealing** temperature
set at 700.degree. C. in a conventional producing method;

DRPR:
FIG. 23 is a graph showing a change in the remanent polarization Pr of a film
relative to the atmospheric gas pressure of a second **annealing** (a second
annealing pressure) of a fourth embodiment of ferroelectric film element

according to the present invention;

DRPR:
FIG. 24 is a graph showing a change in accumulated charge .delta.Q relative to the atmospheric gas pressure of a second **annealing** (a second **annealing** pressure) of the fourth embodiment;

DRPR:
FIG. 25 is a graph showing a change in coercive field Ec relative to the atmospheric gas pressure of a second **annealing** (a second **annealing** pressure) of the fourth embodiment;

DRPR:
FIG. 26 is a graph showing a change in leakage current density under voltage application of 3 V relative to the atmospheric gas pressure of a second **annealing** (a second **annealing** pressure) of the fourth embodiment;

DRPR:
FIG. 27 is an X-ray diffraction pattern of a film relative to the atmospheric gas pressure of a second **annealing** (a second **annealing** pressure) of the SBT film in the fourth embodiment; and

DRPR:
FIG. 28 is a graph showing a change in film composition ratio relative to the atmospheric gas pressure of a second **annealing** (a second **annealing** pressure) of the SBT film in the fourth embodiment.

DEPR:
Then, using the RTA method as a first **annealing**, heat treatment is performed at 600.degree. C. for 30 min in an atmosphere of oxygen under the atmospheric pressure (step S13) and a 200 nm Pt upper electrode 6 is mask-deposited by the EB (Electron Beam) deposition method (step S14). At this first **annealing**, the pyrolysis removal of the organic substances contained in the applied and dried ferroelectric film is performed. And, simultaneously with the

pyrosis removal
of organic substances, the ferroelectric film is partly crystallized, which
seems to act as a kind of nucleus forming process. Meanwhile, with this
embodiment, heat treatment was performed in an atmosphere of oxygen under the
atmospheric pressure by using the RTA method, but a normal heat treatment
furnace may be employed in place of the RTA method and a mixed gas of oxygen
and an inert gas such as nitrogen or argon may be employed as atmosphere gas.
In addition, with this embodiment, a 100 .mu.m.phi. Pt upper electrode was
adopted as the electrode size for estimating the characteristics of
ferroelectrics, but the present invention is not limited to this electrode
size.

DEPR:
Next, after the formation of an upper electrode, a 30 min **annealing** is
performed as a second **annealing** (principal **annealing**) in a 10 Torr atmosphere
of oxygen at 400.degree. C.-750.degree. C. for 30 min by the RTA method (Step
S15). This second **annealing** is for the purpose of a complete **crystallization**
of ferroelectric films. Meanwhile, with this embodiment, **annealing** was
performed in a 10 Torr atmosphere of oxygen by using the RTA method, but a
normal heat treatment furnace may be employed except the RTA method provided
heat treatment can be done in an atmosphere of gas pressure below 1 atm. As
annealing atmosphere, an inert gas such as nitrogen or argon may be employed
and a mixed gas comprising not greater than two sorts of gases out of an inert
gas such as nitrogen or argon and oxygen may be employed.

DEPR:
FIGS. 3, 4 and 5 are graphs showing ferroelectric characteristics of the film
obtained by the above producing steps relative to a second **annealing**

temperature. Measurements of ferroelectric characteristics were made for a
capacitor of the type shown in FIG. 1 with the applied voltage set at 3 V by
using a well known Soya Tower circuit.

DEPR:
FIG. 3 is a graph showing a change in the remanent polarization Pr of a film.
With lowering of the second **annealing** temperature, Pr also decreases, but a
value of more than 4 .mu.C/cm.sup.2 is obtained at a second **annealing**
temperature of even 600.degree. C. FIG. 4 is a graph showing a value of
coercive field Ec for the film produced by this producing method, Ec is almost
constant independent of second **annealing** temperatures above 500.degree. C. As
with Pr shown in FIG. 3, the accumulated charge .delta.Q shown in FIG. 5
increases depending on second **annealing** temperatures and shows a good
characteristic at second **annealing** temperatures of 500.degree. C. or higher.

DEPR:
FIGS. 6, 7 and 8 are graphs showing the applied-voltage dependence of
ferroelectric characteristics for cases where a 30 min **annealing** was made at a
first **annealing** temperature of 600.degree. C. in an atmosphere of oxygen under
the atmospheric pressure and the second **annealing** was performed in a 10 Torr
atmosphere of oxygen at 600.degree. C. for 30 min of **annealing**. These graphs
show values of Pr, Ec and .delta.Q respectively for FIGS. 6, 7 and 8 and reveal
that Pr, Ec and .delta.Q begin to be saturated upward from the order of 3 V in
applied voltage. This shows that constant characteristics are always obtained
at applied voltages of not lower than 3 V and the ferroelectric characteristics
can be said to be good.

DEPR:
FIG. 9 is a graph in which a change in accumulated charge

.delta.Q relative to number of repeated polarization reversals is plotted for cases where polarization reversals were made under application of a 3 V and 1 MHz pulse to a sample on which a 30 min **annealing** was performed at a second **annealing** temperature of 600.degree. C. in an atmosphere of oxygen under the atmospheric pressure and a 30 min **annealing** was performed at a first **annealing** temperature of 600.degree. C. in a 10 Torr atmosphere of oxygen. Even after 2.times.10.sup.11 cycles of polarization reversals, **no** change whatever is observed in accumulated charge and a good characteristic is indicated in application to a nonvolatile memory.

DEPR:
FIG. 10 is a graph showing a change in leakage current density relative to a second **annealing** temperature under application of 3 V. For 550.degree. C. or higher, a value of 6-9.times.10.sup.-8 A/cm.sup.2 is obtained independently of second **annealing** temperatures, whereas the leakage current density is large for 500.degree. C. or lower but **no** such increase in leakage that formerly became at issue for a lower second **annealing** temperature was observed.

DEPR:
FIG. 11 is a surface SEM photograph of a film after a 30 min **annealing** made at a first **annealing** temperature of 600.degree. C. in an atmosphere of oxygen under the atmospheric pressure and a 30 min **annealing** made at a second **annealing** temperature of 600.degree. C. in a 10 Torr atmosphere of oxygen and reveals that the film forms a fine-structured film comprising globular crystal grains of 700 .ANG. or smaller. In addition, also for a second **annealing** temperature of 650.degree. C., a fine-structured film comprising globular crystal grains of 700 .ANG. or smaller was formed as with a second temperature of 600.degree. C. On the other hand, when a 30 min **annealing** was

made at a
first **annealing** temperature of 600.degree. C. in an atmosphere of oxygen under
the atmospheric pressure and a 30 min **annealing** was made at a second **annealing**
temperature of 700.degree. C. in a 10 Torr atmosphere of oxygen, the SBT film
obtained was strap-like and comprised crystal grains of 500-5000 .ANG. size,
and still greater crystal grains were obtained for a second **annealing**
temperature of 750.degree. C. than those for a second **annealing** temperature of
700.degree. C. From these, it is concluded that the maximum crystal grain size
of crystal particles constituting the SBT film increases with rising second
annealing temperature and a fine-structured film comprising globular crystal
grains of 700 .ANG. size or smaller can be formed for second **annealing**
temperatures of 650.degree. C. or lower.

DEPR:
From a result of X-ray diffraction, polycrystals of SrBi.sub.2 Ta.sub.2 O.sub.9
were found for second **annealing** temperatures of 500.degree. C. or higher, but
no clear crystal could be confirmed for second **annealing** temperatures of
450.degree. C. or higher.

DEPR:
In production of a ferroelectric element for this control, the difference from
that of the first embodiment mentioned above lies only in the step of second
annealing at the formation of the SBT film. That is, to an SBT film with a 100
.mu.m.phi. Pt top electrode 6 mask-deposited thereon as with the first
embodiment mentioned above, a 600-750.degree. C. and 30 min **annealing** was
performed as the second **annealing** in an atmosphere of oxygen under the
atmospheric pressure by using the RTA method in the control (Step S20).

DEPR:

FIGS. 13, 14 and 15 are graphs showing ferroelectric characteristics of the
film obtained in the process of this control relative to a second **annealing**
temperature. As with the first embodiment mentioned above, measurements of
ferroelectric characteristics were made for a capacitor of the type shown in
FIG. 1 with the applied voltage set at 3 V by using a well known Soya Tower
circuit.

DEPR:
FIG. 13 is a graph showing a change in the remanent polarization Pr of a film.
With lowering of the second **annealing** temperature, a value of Pr abruptly
decreased beyond the boundary of 730.degree. C., became very small like 2
.mu.C/cm.sup.2 or less at 700.degree. C. or lower and hardly any ferroelctricity was exhibited at 600.degree. C. This will be compared with the
result of the first embodiment mentioned above. In the first embodiment, it
sufficed to obtain a value of Pr not less than 4 .mu.C/cm.sup.2 that the second
annealing temperature is 600.degree. C. (cf. FIG. 3), whereas a value of Pr
not less than 4 .mu.C/cm.sup.2 is found to be not obtainable in the control
unless the second **annealing** temperature is 730.degree. C. or higher. From
these, it is clear that lowering of second **annealing** temperature can be
implemented to obtain the equivalent value of Pr in the first embodiment as
compared with the control.

DEPR:
FIG. 14 is a graph showing a value of coercive field Ec and Ec exhibits an
almost constant value independently of second **annealing** temperatures at
650.degree. C. or higher. As with Pr shown in FIG. 13, the accumulated charge
.delta.Q shown in FIG. 15 abruptly decreases for lower second **annealing**
temperatures than the boundary of 730.degree. C.

DEPR:
FIG. 16 is a graph showing a change in leakage current density relative to
second **annealing** temperatures under application of 3 V. For each decrease of
50.degree. C. in second **annealing** temperature, the leakage current density
increases by one decimal unit and indicates a decreasing tendency at
600.degree. C., but the SBT film of 600.degree. C. exhibits hardly any
ferroelectricity.

DEPR:
FIG. 17 is a surface SEM photograph of a film after a 30 min **annealing** made at
a first **annealing** temperature of 600.degree. C. in an atmosphere of oxygen
under the atmospheric pressure and a 30 min **annealing** made at a second
annealing temperature of 700.degree. C. in an atmosphere of oxygen under the
atmospheric pressure. The SBT film obtained in this case was strap-like and
comprised crystal grains of 1500-9000 .ANG. size.

DEPR:
Here, the size of crystal grains will be compared between the first embodiment
mentioned above and the control. As mentioned before, in the SBT film for a 30
min **annealing** made at a first **annealing** temperature of 600.degree. C. in an
atmosphere of oxygen under the atmospheric pressure and a 30 min **annealing** made
at a second **annealing** temperature of 700.degree. C. in a 10 Torr atmosphere of
oxygen, the crystal grain size ranged from 500 .ANG. to 5000 .ANG., whereas
the crystal grain size ranged from 1500 .ANG. to 9000 .ANG. in this control
as mentioned above. Smaller crystal grains are obtained for the first
embodiment than those of the control. Thus, comparative study of these SBT
films differing only in the second **annealing** temperature reveals that a fine
structurization of the film can be achieved by performing a second **annealing** in

the atmosphere of gas pressure not higher than 1 atm.

DEPR:
Next, between the above first embodiment and the control, comparative study will be made of the size of crystal grains in a ferroelectric film that yields a nearly equal value of remanent polarization Pr. In an SBT film according to the above first embodiment for cases where a 30 min **annealing** was performed at a first **annealing** temperature of 600.degree. C. in an atmosphere of oxygen under the atmospheric pressure and a 30 min **annealing** was performed at a second **annealing** temperature of 600.degree. C. in a 10 Torr atmosphere of oxygen, a value of Pr was about 4.2 .mu.C/cm.sup.2 as shown in FIG. 3 and crystal grains were 700 .ANG. or smaller in size. On the other hand, as an SBT film yielding a nearly equal value of Pr in the control, there is mentioned a case where a 30 min **annealing** was made at a first **annealing** temperature of 600.degree. C. in an atmosphere of oxygen under the atmospheric pressure and a 30 min **annealing** was made at a second **annealing** temperature of 730.degree. C. in an atmosphere of oxygen under the atmospheric pressure and a value of Pr=about 4.3 .mu.C/cm.sup.2 was obtained (cf. FIG. 13). Observation of this SBT film revealed that the size of crystal grains was 1500-9000 .ANG.. From comparison it is found that smaller crystal grains are obtained for the first embodiment than those of the control. From this, it is clear also in comparison of SBT films yielding a nearly equal value of Pr that a fine structurization of the film can be achieved by performing a second **annealing** in the atmosphere of gas pressure not higher than 1 atm.

DEPR:
The result of X ray diffraction in the control shows that polycrystals of SrBi.sub.2 Ta.sub.2 O.sub.9 was formed for second **annealing**

temperatures of
650.degree. C. or higher but **no** clear crystallization could not be confirmed
for second **annealing** temperatures of 600.degree. C. or lower.

DEPR:
Like these, in a conventional producing method, an abrupt decrease in values of
Pr and .delta.Q and an increase in leakage current were observed with lowering
second **annealing** temperature and **annealing** of 730.degree. C. or higher was
required for application to ferroelectric memories. According to the first
embodiment of the present invention, however, the second **annealing** made in an
atmosphere of gas pressure not higher than 1 atm permits not only an abrupt
increase in values of Pr and .delta.Q but also an increase in leakage current
to be suppressed. Consequently, sufficient characteristics can be obtained as
ferroelectric memories at a maximum **annealing** temperature of 650.degree. C.
and it becomes possible to adopt a stack structure necessary for the highly
integrated FRAM. In addition, a producing method according to this embodiment
enables coarser crystal grains to be suppressed, thereby implementing a
fine-structured film and an even surface, and leakage current to be reduced and
moreover is suitable for a fine machining and for the production of a
high-density device.

DEPR:
Next, as shown in FIG. 19b, after a TiN barrier metal layer 46 is deposited in
a film thickness of 2000 .ANG. by the well known sputtering method, a Pt film
47 is deposited in a film thickness of 1000 .ANG. to make a bottom electrode.
On this bottom electrode, an SrBi.sub.2 Ta.sub.2 O.sub.9 film (hereinafter,
referred to as SBT film) is scheduled to be formed as ferroelectric film 48,
but description will be omitted of a synthesis method for the precursor
solution employed for the formation of an SBT film and the steps

leading to the
first **annealing** in the process for forming an SBT film by using this precursor
solution because they are the same as the steps extending from the step S1 to
the step S13.

DEPR:
The SBT film 48, the Pt bottom electrode 47 and the TiN barrier metal layer 46
after the first **annealing** are machined to the size of 3.0 .mu.m square by the
well known photolithography method and dry etching method to make such a shape
as shown in FIG. 19b. For dry etching, an ECR etcher is employed and the gas
species used are a gas mixture comprising **Ar**, Cl.sub.2 and CF.sub.4 for the SBT
film, a gas mixture comprising C.sub.2 F.sub.6, CHF.sub.3 and Cl.sub.2 for the
Pt bottom electrode and Cl.sub.2 gas for the TiN barrier metal. At this time,
since the SBT film and Pt bottom electrode are very fine in structure and even,
a precise micro-machining is executable and the CD loss can be suppressed to
0.1 .mu.m or smaller.

DEPR:
Next, as shown in FIG. 19d, after a 1000 .ANG. Pt upper electrode is formed by
the well-known sputtering method and is machined to a plate wire 49 by the well
known photolithography method and dry etching method, a 600.degree. C. and 30
min heat treatment is performed as the second heat treatment by the RTA method
to crystallize an SBT film. The section of the SBT film after **crystallization**
was yet very smooth and fine-structured and did not injure the shape of a
ferroelectric capacitor. Meanwhile, the film thickness of the SBT film was
measured to be 2000 .ANG..

DEPR:
FIG. 21 is a graph in which a change in accumulated charge .delta.Q relative to
number of polarization reversals is plotted for cases where polarization

reversals were made under application of a 3 V and 1 MHz pulse. Even after
2.times.10.sup.11 cycles of polarization reversals, **no** change whatever is
observed in accumulated charge and a good characteristic is indicated as
nonvolatile memory.

DEPR:
With respect to the third embodiment of ferroelectric film element having a
capacitor structure, FIG. 22 shows variations in accumulated charge .delta.Q
relative to the maximum crystal grain size of an SBT film when measured at 100
places of a 2 .mu.m square Pt top electrode. In FIG. 22, the ordinate
represents a value of the standard deviation (.sigma.) of accumulated charge
.delta.Q divided by the average (.delta.Q.sub.AVE) of accumulated charge
.delta.Q and the abscissa represents the maximum crystal grain size of an SBT
film. FIG. 22 reveals that .sigma./.delta.Q.sub.AVE is 10% or less for films
of maximum crystal grain size not greater than 1000 .ANG. and variations of
accumulated charge .delta.Q are very small but a value of
.sigma./.delta.Q.sub.AVE is so large that a stable characteristic is hardly
attainable. Thus, when the second **annealing** temperature is 650.degree. C. or
lower, as described for the first embodiment, since a fine-structured film
having a maximum crystal grain size of 700 .ANG. or smaller is obtained, the
obtained film is found to have hardly any variation and be good in
ferroelectric characteristics. From this it is concluded that the second
annealing temperature is preferably in the range of 500.degree. C.-650.degree.
C. for obtaining an SBT film of a small variation in characteristics.

DEPR:
Hereinafter, a fourth embodiment according to the present invention will be
described referring to the drawings. With the fourth embodiment, in the step

S15 of FIG. 2 shown for the above first embodiment, the RTA method was employed and a 600.degree. C. and 30 min **annealing** was made in a 1-760 Torr atmosphere of oxygen as second **annealing** (principal **annealing**) but otherwise for the structure of a ferroelectric element, other producing steps and the like, the fourth embodiment is quite the same as the first embodiment. Incidentally, the reason why the atmosphere gas pressure of the second **annealing** (second **annealing** pressure) is set at the range of 1-760 Torr is that the lower limit is chosen at 1 Torr at which the formed SBT film indicated hardly any ferroelectricity and the upper limit is chosen at 760 Torr equal to the atmospheric pressure.

DEPR:
FIGS. 23, 24 and 25 are graphs showing ferroelectric characteristics of the film obtained in the producing steps mentioned above relative to atmosphere gas pressure of the second **annealing** (second **annealing** pressure). Measurements of ferroelectric characteristics were made for a capacitor of the type shown in FIG. 1 with the applied voltage set at 3 V by using a well known Soya Tower circuit.

DEPR:
FIG. 23 is a graph showing values of remanent polarization Pr relative to atmosphere gas pressure of the second **annealing** (second **annealing** pressure). At an atmosphere gas pressure of 760 Torr, hardly any ferroelectricity was exhibited but a value of Pr increases with lowering gas pressure, reaches a maximum near a pressure of 5 Torr and decreases with a further lowering of gas pressure. At a gas pressure of 5 Torr, the remanent polarization Pr was 5.5 .mu.C/cm.sup.2 and the coercive field Ec was 25 kV/cm, so that sufficient characteristics were obtained as ferroelectric capacitor. In addition, from

FIG. 23 Pr is found to be 2.5 .mu.C/cm.sup.2 or greater if the atmosphere gas pressure of the second **annealing** (second **annealing** pressure) is in the range of 2 Torr-20 Torr, which exhibits a sufficient ferroelectric characteristic.

DEPR:
FIG. 24 is a graph showing values of accumulated charge .delta.Q relative to atmosphere gas pressure of the second **annealing** (second **annealing** pressure). As with remanent polarization Pr, a value of accumulated charge .delta.Q increases with lowering atmosphere gas pressure from 760 Torr, reaches a maximum near a pressure of 5 Torr and decreases with a further lowering of gas pressure. At a gas pressure of 5 Torr, an excellent value of 10.2 .mu.C/cm.sup.2 was obtained as accumulated charge .delta.Q. In addition, generally for a ferroelectric memory at an integrated degree of Mbit class, an accumulated charge of 5 .mu.C/cm.sup.2 or greater is required. Accordingly, it is found from FIG. 24 that the accumulated charge .delta.Q is 5 .mu.C/cm.sup.2 or greater for the range of 2 Torr-20 Torr and a memory produced in this range of pressure can acquire a sufficient accumulated charge .delta.Q needed as a ferroelectric memory at an integrated degree of Mbit class. Furthermore, as a result of observing the SBT film produced under this second **annealing** pressure, the SBT film can be confirmed to be fine-structured and have a good surface evenness.

DEPR:
FIG. 25 is a graph showing a value of coercive field Ec relative to atmosphere gas pressure of the second **annealing** (second **annealing** pressure). For second **annealing** pressure ranging from 2 Torr to 200 Torr, Ec exhibits an almost constant value in the neighborhood of 25 kV/cm.

DEPR:

FIG. 26 is a graph showing a change in leakage current density relative to atmosphere gas pressure of the second **annealing** (second **annealing** pressure) under application of 3 V. For any value of second **annealing** pressure, good values of leakage current density on the order of 10.sup.-7 to 10.sup.-8 are obtained.

DEPR:
FIG. 27 is an X ray diffraction pattern of a film relative to atmosphere gas pressure of the second **annealing** (second **annealing** pressure). In FIG. 27, a, b, c, d, e and f denotes that the second **annealing** pressure is 760 Torr, 200 Torr, 20 Torr, 10 Torr, 2 Torr and 1 Torr, respectively. Meanwhile, in FIG. 27, the abscissa denotes a diffraction angle 2.theta. (deg) and the ordinate denotes diffraction intensity (arbitrary intensity). Concerning the ordinate, a position at which the diffraction intensity=0 is moved for each second **annealing** pressure. And in FIG. 27, SBT (008), SBT (105), SBT (110) and SBT (200) denote diffraction peaks originating from SrBi.sub.2 Ta.sub.2 O.sub.0 (SBT), .delta.-TaO (001) and .delta.-TaO (002) denote diffraction peaks originating from .delta. phase TaO, Si denotes diffraction peaks originating from the silicon substrate and Pt denotes diffraction peaks originating from the Pt lower electrode.

DEPR:
According to FIG. 27, polycrystalline peaks of SBT (SBT (008), SBT (105), SBT (110) and SBT (200)) appear for 2 Torr to 200 Torr, whereas **no** SBT peak but TaO peaks (.delta.-TaO (001) and .delta.-TaO (002)) appear for 1 Torr. And for 760 Torr, SBT peaks are very broad and therefore an amorphous film is thought to be formed. Observed results of this X ray diffraction reveals that a film exhibiting SBT peaks was obtained for atmosphere gas pressure ranging from 2

Torr to 200 Torr.

DEPR:
FIG. 28 is a graph showing a change in film composition ratio relative to
atmosphere gas pressure of the second **annealing** (second **annealing** pressure).
Since the result of EPMA measurements concerning the SBT film compositions
reveals that, whereas the Ta composition and Sr composition were nearly
constant independently of second **annealing** pressure, the Bi composition changed
depending on second **annealing** pressure, FIG. 28 is a graphic representation of
composition ratios Bi/Ta and Sr/Ta. According to FIG. 28, a value of Bi/Ta is
much the same as the composition ratios of raw material stock (Bi/Ta=2.4/2=1.2)
at 750 Torr, gradually decreases with lowering of second **annealing** pressure
till 2 Torr and becomes stoichiometric (Bi/Ta=1.0) near 5 Torr.

DEPR:
And at a second **annealing** pressure of 1 Torr, a value of Bi/Ta abruptly
decreases. Such a change in Bi composition is attributable to volatilization
of Bi or diffusion of Bi to electrodes at the time of second **annealing** and such
a large shift of Bi composition is considered to be a cause for the fact that
hardly any ferroelectricity was obtained at a second **annealing** pressure of 1
Torr. On the other hand, since the Ta composition and Sr composition were
almost constant independently of second **annealing** pressure as mentioned above,
Sr/Ta was also nearly constant and was much the same as the composition ratio
of raw material stock (Sr/Ta=1/2=0.5).

DEPR:
To be more specific, though hardly any **crystallization** was made at **annealing**
temperatures of 650.degree. C. or lower and moreover **annealing** of 730.degree.
C. or higher was required for obtaining characteristics needed as **ferroelectric**

memories in a conventional producing method, a producing method according to
the present invention enables the **annealing** temperature to be lowered by
100.degree. C. or more and permits sufficient characteristics as memory to be
obtained at as low **annealing** temperature as 600.degree. C., so that
integration of **ferroelectric** memories using a stack structure becomes possible.

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US006060735A

United States Patent [19]

Izuha et al.

[11] Patent Number: 6,060,735

[45] Date of Patent: May 9, 2000

[54] THIN FILM DIELECTRIC DEVICE

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[73] Assignee: Kabushiki Kaisha Toshiba, Japan

[21] Appl. No.: 08/923,123

[22] Filed: Sep. 4, 1997

[30] Foreign Application Priority Data

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Jan. 30, 1997 [JP] Japan 9-017047

[51] Int. Cl.[7] H01L 29/78; H01L 33/00

[52] U.S. Cl. 257/295; 257/296

[58] Field of Search 257/295, 296

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Primary Examiner—Stephen D. Meier
Attorney, Agent, or Firm—Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P.

[57] ABSTRACT

A thin film dielectric device is disclosed, that comprises a substrate, a lower electrode formed on the substrate and composed of a laminate film having columnar grains that have grown in a vertical to a surface of the substrate, a dielectric thin film formed on the lower electrode and composed of a perovskite oxide, the dielectric thin film being a polycrystalline film having columnar grains that have successively grown from the columnar grains of the lower electrode and that takes over a crystal orientation of the lower electrode, the lattice constant of the lower electrode being matched with the lattice constant of the dielectric thin film at the interface therebetween with the columnar grains, and an upper electrode formed on the dielectric thin film. The lattice matching of the columnar grains solves problems of the increase of the leak current of the thin film dielectric device and the degradation of the dielectric breakdown resistance. In addition, the polycrystalline film having the columnar grains that succeed at the interface of the electrode/dielectric thin film can be properly formed on the semiconductor substrate such as Si substrate. Thus, the thin film dielectric device according to the present invention can be applied to a real LSI circuit and so forth.

22 Claims, 5 Drawing Sheets

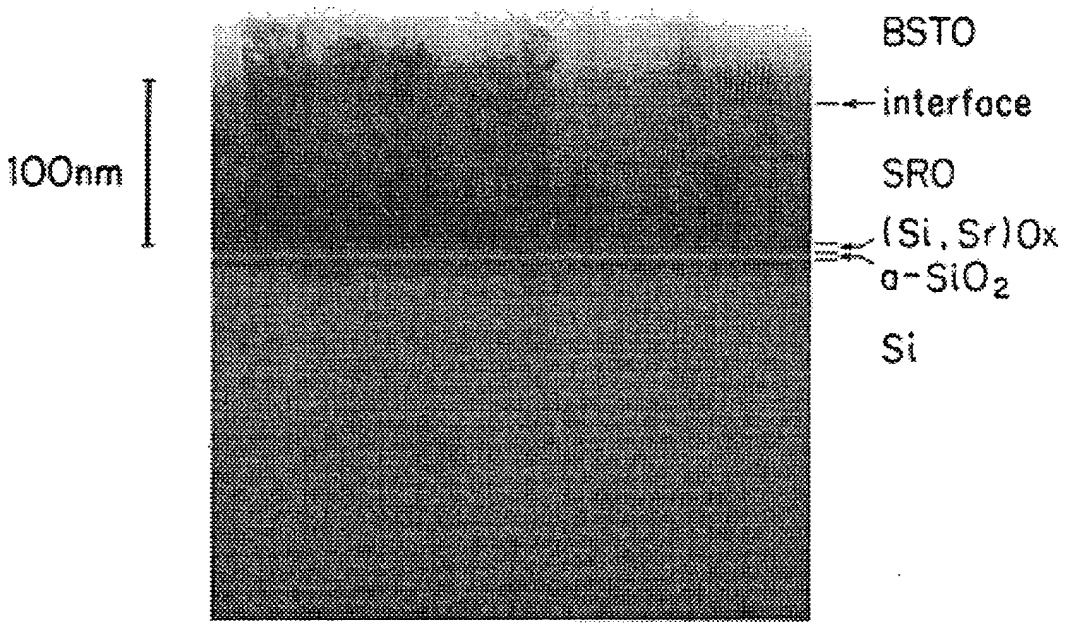


FIG. 1

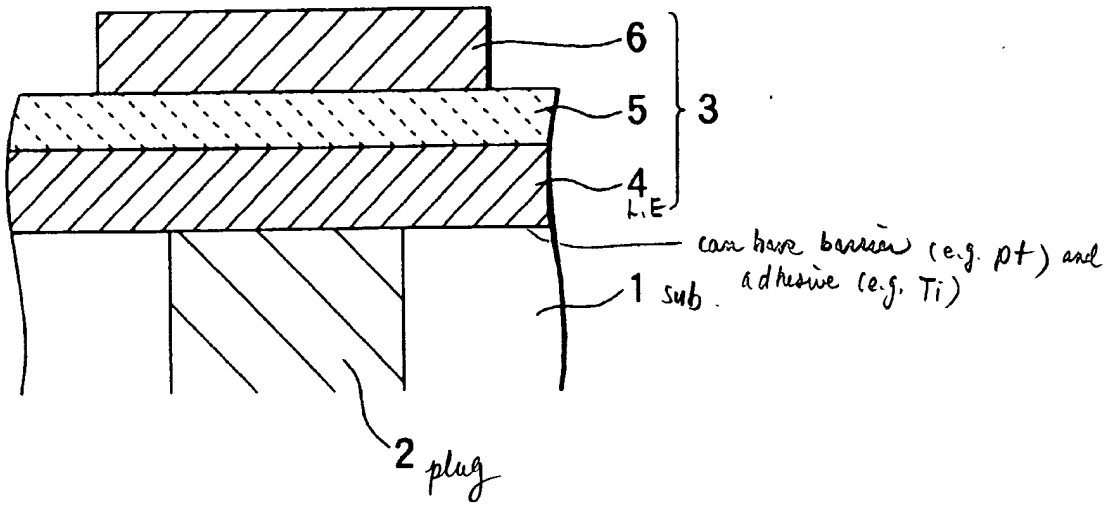

6
5
3
4
L.E
can have barrier (e.g. Pt) and adhesive (e.g. Ti)
1 sub
2 plug

FIG. 2

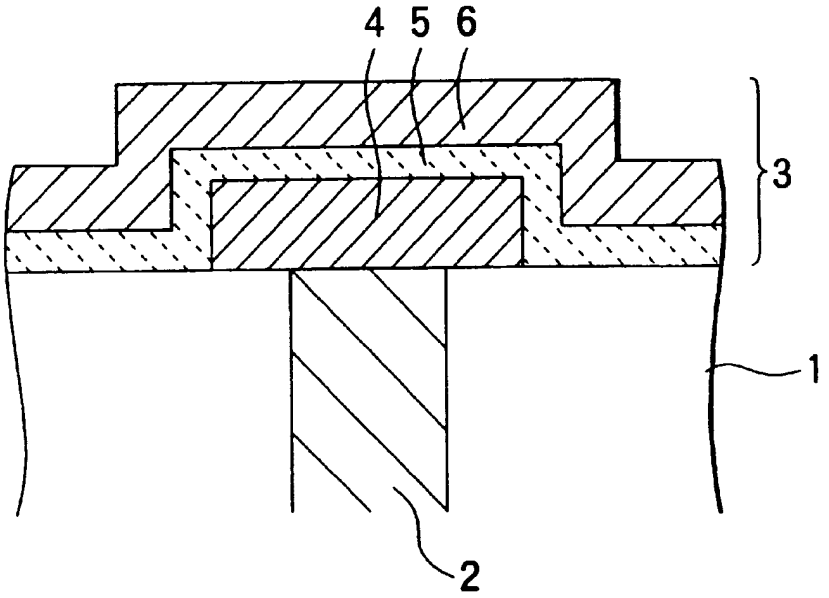

4 5 6
3
1
2

FIG. 3

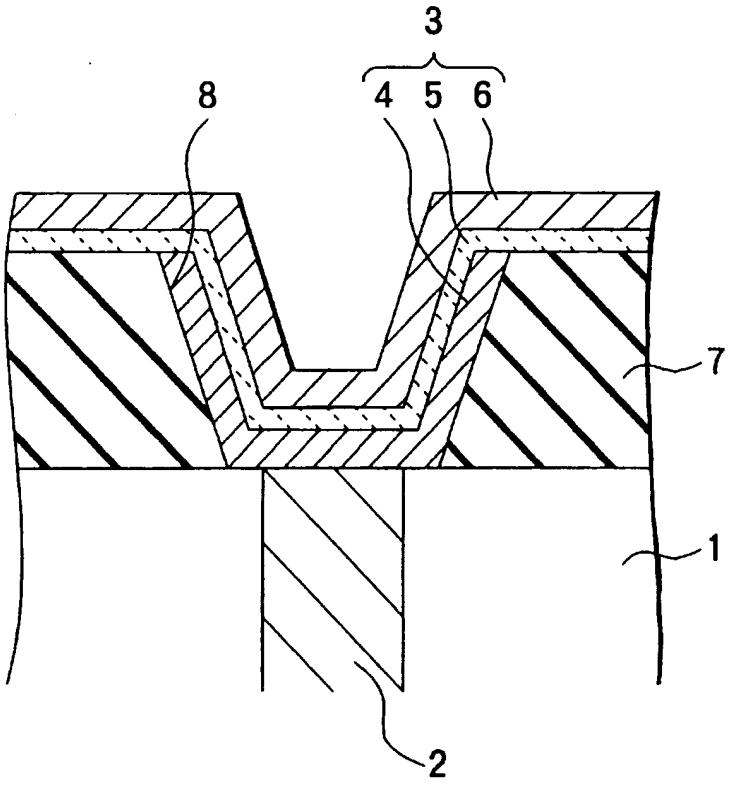

3
8
4 5 6
7
1
2

FIG. 4A

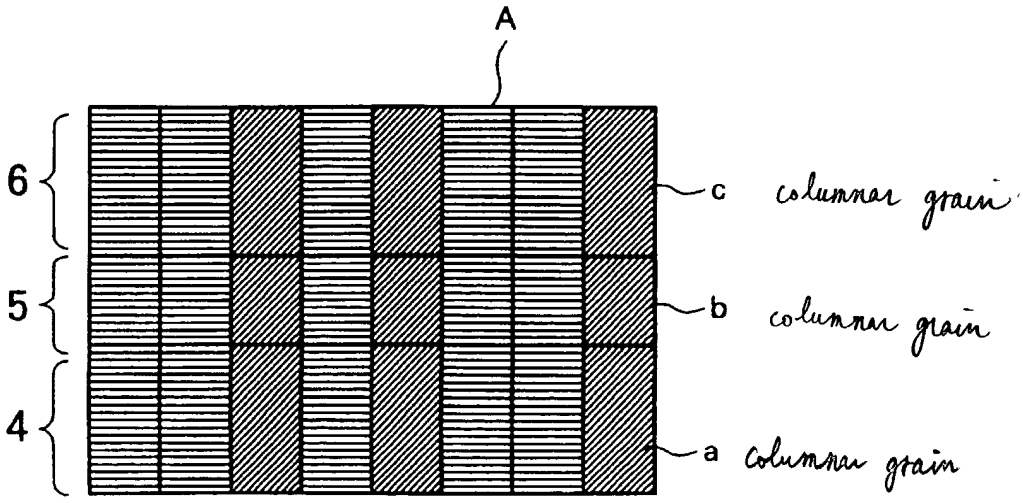

A
6
5
4
c columnar grain
b columnar grain
a columnar grain

FIG. 4B

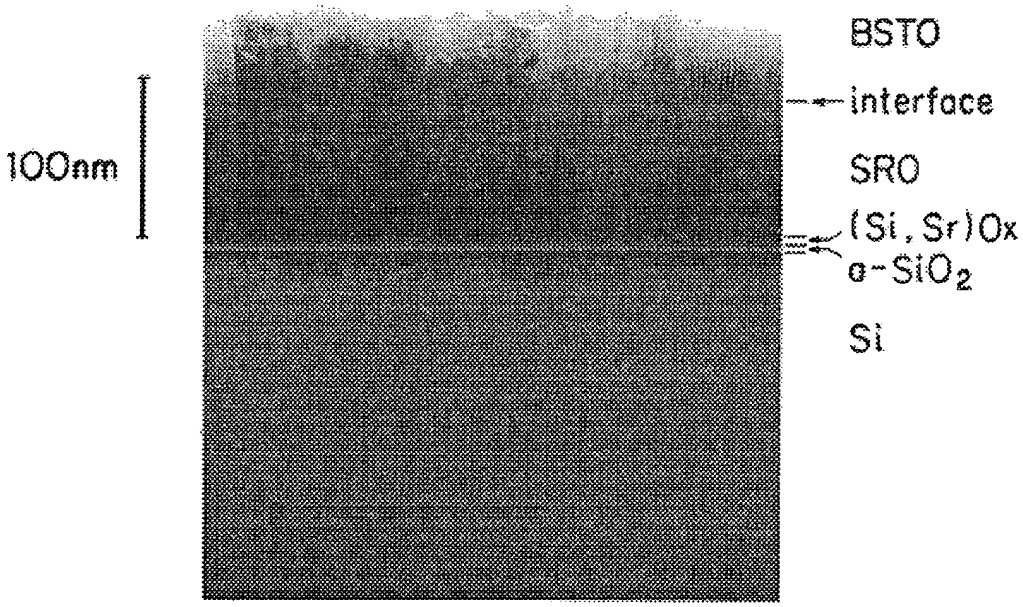


FIG. 5

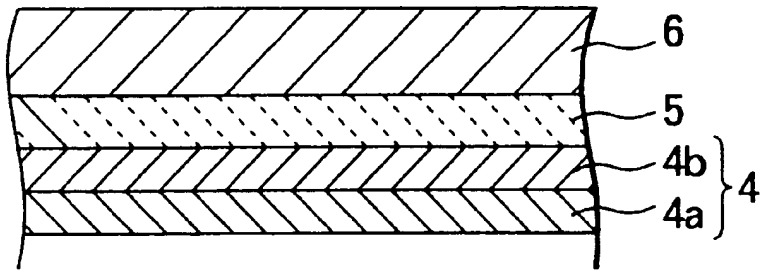


FIG. 6

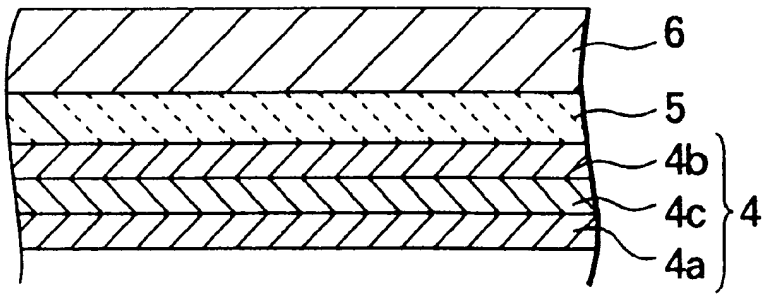


FIG. 7

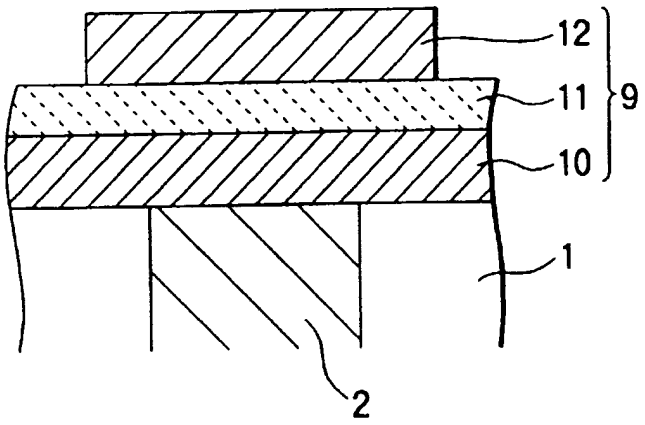
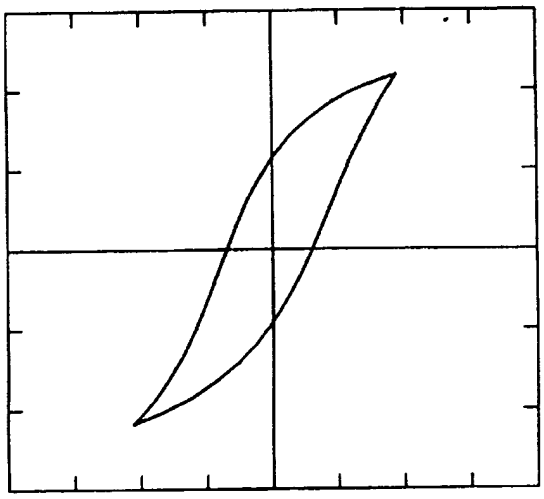


FIG. 8



AXIS X : 20MV/mdiv

AXIS Y : 0.1C/m^2 div

THIN FILM DIELECTRIC DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a thin film dielectric device having a dielectric thin film composed of a perovskite oxide.

2. Description of the Related Art

In recent years, materials with high permittivity and ferroelectricity of thin film dielectric devices (thin film capacitors) that are disposed on large storage DRAMs and non-volatile ferroelectricity memories (FRAMs) and device structures thereof have been intensively studied. For example, the dielectric constants of perovskite oxides such as $SrTiO_3$ (hereinafter referred to as STO) and $Ba_{1-x}Sr_xTiO_3$ (hereinafter referred to as BSTO) are much larger than the dielectric constants of conventional materials such as SiO_2, Si_3N_4, and Ta_2O_5. Thus, even if memory cells are finely structured, a sufficient storage capacity of electric charges can be obtained. In addition, a desired storage capacitance can be accomplished without need to use a complicated capacitor structure.

In a thin film dielectric device having a dielectric thin film composed of a perovskite oxide, it is considered that a noble metal such as Pt or Ru, an oxide of such as Ru, or a laminate film thereof to be a lower electrode. Among them, Ru has an excellent machinability and can be finely patterned by reactive ion etching (RIE) method or the like. Thus, it was considered that Ru is an excellent material of a capacitor electrode.

However, in a thin film dielectric device of which Ru or an oxide thereof is used for a lower electrode, a large amount of interface levels will take place due to ion defeats resulting from the mismatching of the interface an electrode and a dielectric thin film. The interface levels causes a leak current to increase and a dielectric breakdown resistance to decrease.

On the other hand, it is considered to use a conductive perovskite oxide having the same crystal structure as the above-described STO and BSTO for the material of an electrode, in particular, for the material of a lower electrode. When a conductive perovskite oxide is used for a lower electrode and it is epitaxially grown from the lower electrode to a dielectric thin film composed of the perovskite oxide or to an upper electrode, the lower electrode and the dielectric thin film are highly matched at the interface thereof. In addition, the dielectric thin film and the upper electrode are highly matched at the interface thereof. It is expected that such an epitaxially grown film suppresses the leak current due to a large amount of interface levels from increasing and the dielectric breakdown resistance from degradation.

To actually fabricate a thin film dielectric device that is epitaxially grown, a single crystal substrate composed of MgO or $SrTiO_3$ should be used for a substrate. However, in a real LSI circuit or the like, the lower electrode should be formed on a plug composed of poly-silicon or tungsten (Si plug or W plug). It is very difficult to epitaxially grow the lower electrode composed of a conductive perovskite oxide on a plug composed of poly-silicon in a good condition. Thus, the electrode and the dielectric thin film cannot be highly matched at the interface thereof.

On the other hand, it is considered to use a polycrystalline film composed of a conductive perovskite oxide for a lower electrode. For example, a structure of which a polycrystalline film composed of a conductive perovskite oxide such as $SuRuO_3$ is formed on a plug composed of poly-silicon or the like through a barrier metal layer composed of such as TiN as a lower electrode and then a dielectric thin film composed of for example BSTO is formed on the polycrystalline film has been considered. However, in such a structure, the morphology degrades at the interface of the lower electrode and the dielectric thin film and at the interface of the dielectric thin film and the upper electrode. The degradation of the morphology at the interface causes the leak current to increase or a capacitor to short-circuit.

As described above, in a conventional thin film dielectric device having a dielectric thin film composed of perovskite oxide, when a noble metal such as Ru or an oxide thereof is used for a lower electrode, since the dielectric thin film and the lower electrode are not matched at the interface thereof, the leak current increases or the dielectric breakdown resistance decreases.

When the conductive perovskite oxide is used for the lower electrode and epitaxially grown, the substrate thereof is restricted. Thus, an epitaxial film of the conductive perovskite oxide cannot be used for a real LSI circuit or the like due to restrictions on process and device structure. When a polycrystalline film of the conductive perovskite oxide is used for the lower electrode, the morphology degrades at the interface thereof. The degradation of the morphology at the interface causes the leak current to increase or a capacitor to short-circuit.

Thus, in the thin film dielectric device having the dielectric thin film composed of the perovskite oxide, the lattice constant of the electrode and the lattice constant of the dielectric thin film should be highly matched. In addition, when the conductive perovskite oxide is used for the electrode, the flatness of the surface of the polycrystalline film should be improved. Thus, the problems of which the leak current increases and the dielectric breakdown resistance decreases should be solved. In addition, such a thin film dielectric device should be applied to a real LSI or the like.

SUMMARY OF THE INVENTION

Thus, an object of the present invention is to provide a thin film dielectric device that allows the lattice constant of an electrode and the lattice constant of a dielectric thin film to be highly matched so as to suppress a leak current from increasing and a dielectric breakdown resistance from decreasing. Another object of the present invention is to provide a thin film dielectric device that can be applied to a real LSI or the like. A further object of the present invention is to provide a thin film dielectric device having a polycrystalline film of a conductive perovskite oxide with high surface flatness so as to suppress the morphology at the interface of an electrode and a dielectric thin film from degrading, thereby suppressing a leak current from increasing and a dielectric breakdown resistance from decreasing.

The present invention is a thin film dielectric device that comprises a substrate having a capacitor surface, a lower electrode formed on said substrate and composed of a polycrystalline film having columnar grains that have grown in a vertical direction to a capacitor surface of said substrate, a dielectric thin film formed on said lower electrode and composed of a perovskite oxide, said dielectric thin film being a polycrystalline film having columnar grains that have successively grown from the columnar grains of said lower electrode and that takes over a crystal orientation of said lower electrode in each of said columnar grains of said

dielectric thin film, the lattice constant of said dielectric thin film being in each of said columnar grains thereof substantially matched with the lattice constant of said lower electrode at the interface with the columnar grains of said lower electrode, and an upper electrode formed on said dielectric thin film.

Namely, the microstructure of said capacitors can be described as follows.

Said bottom electrode film and said dielectric film are composed of continuous columnar grains and bottom electrode and dielectric share each column at the interface of dielectrics and bottom electrode in each column, the crystallographic relation between dielectric and electrode material is epitaxial: the crystal lattice is continuous and dielectric and electrode crystals share crystallographic axes.

The conductive perovskite oxide electrode formed immediately on a substrate, a plug, or the like or through a barrier metal is a polycrystalline having columnar grains. When the mismatch of the lattice constant of the dielectric composed of a perovskite oxide formed on the conductive perovskite oxide electrode and the lattice constant of the dielectric is in a predetermined range, the dielectric layer grows taking over the columnar grains of the lower electrode. In such a laminate film, the crystal orientation is also taken over. In the columnar grains, the interface of the lower electrode and the dielectric thin film epitaxially grows. The interface is almost free of ion defects and electronic interface levels. Such a local expitaxial structure can be formed at not only the interface of the lower electrode and the dielectric thin film, but the interface of the dielectric thin film and the upper electrode composed of the conductive perovskite oxide. After all, the local expitaxial structure is further effective when it is applied to both the interface of the upper electrode and the dielectric thin film and the interface of the lower electrode and the dielectric thin film.

In the thin film dielectric device according to the present invention, the laminate film portion of the electrode and the dielectric thin film is a polycrystalline film having columnar grains with a local epitaxial structure. Since the lattice constant of the electrode and the lattice constant of the dielectric thin film are matched in the columnar grains, a large amount of interface levels due to ion defects can be suppressed. Consequently, an excessive leak current and a dielectric breakdown resistance can be suppressed. In addition, since the thin film dielectric device according to the present invention is composed of a polycrystalline film, it can be formed on a variety of substrates for real LSIs and so forth.

These and other objects, features and advantages of the present invention will become more apparent in light of the following detailed description of best mode embodiments thereof, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

FIG. **1** is a sectional view showing the structure of a thin film dielectric device according to an embodiment of the present invention;

FIG. **2** is a sectional view showing another example of the structure of the thin film dielectric device shown in FIG. **1**;

FIG. **3** is a sectional view showing a further example of the structure of the thin film dielectric device shown in FIG. **1**;

FIG. **4A** is a schematic diagram showing a fine structure of a thin film dielectric device according to the present invention;

FIG. **4B** is a photo taken by a microscope (TEM) showing a fine structure of the thin film dielectric device according to the present invention;

FIG. **5** is a sectional view showing an example of the structure of a lower electrode of the thin film dielectric device shown in FIG. **1**;

FIG. **6** is a sectional view showing another example of the structure of the lower electrode of the thin film shown in FIG. **1**;

FIG. **7** is a sectional view showing the structure of a thin film dielectric device according to another embodiment of the present invention; and

FIG. **8** is a hysteresis curve of polarization and electric field (P-E) of a thin film dielectric device fabricated according to twentieth embodiment.

DESCRIPTION OF PREFERRED EMBODIMENTS

Next, embodiments of the present invention will be described.

FIG. **1** is a sectional view showing the structure of a thin film dielectric device according to an embodiment of the present invention. In FIG. **1**, reference numeral **1** is a substrate having a conductor layer such as a plug **2**. An example of the substrate **1** is a semiconductor substrate. The plug **2** is composed of a poly-silicon (poly-Si), tungsten (w), and so forth. A thin film dielectric device **3** is formed on the conductor layer such as the plug **2**. The thin film dielectric device **3** is used for an electric charge storing portion of a semiconductor memory device such as DRAM or FRAM.

In the above-described thin film dielectric device **3**, reference numeral **4** is a lower electrode. A dielectric thin film **5** composed of a perovskite oxide with a film thickness of 10 to 100 nm is formed on the lower electrode **4**. An upper electrode **6** is disposed on the dielectric thin film **5**. A barrier layer may be disposed between the plug **2** and the lower electrode **4**. The barrier layer prevents the lower electrode **4** from reacting with Si and W. In addition, the barrier layer prevents Si and W from diffusing. The material of the barrier layer is for example a noble metal such as Pt or Ru or an oxide of Ru. In addition, an adhesion layer may be disposed so as to improve adhesive characteristic. The adhesion layer is composed of Ta, TiN, $Ti_{1-x}Al_xN$, or the like.

Depending on the application of the thin film dielectric device **3**, a relevant perovskite oxide having the function of dielectric is used. For example, when the thin film dielectric device **3** is used for a capacitor of a DRAM, a high dielectricity perovskite oxide such as $SrTiO_3$ (STO) or $Ba_{1-x}Sr_xTiO_3$ (BSTO) is used. When the thin film dielectric device **3** is used for an FRAM, a ferroelectric perovskite oxide such as $Pb(Zr,Ti)O_3$ (PZT), $(Pb,La)(Zr,Ti)O_3$ (PLZT), Bi—Sr—Ta—O, or Bi—Sr—Ti—O is used. As will be described later, with the dielectric thin film **5** composed of BSTO or the like that has distortion induced ferroelectricity, an electric charge storing portion of an FRAM can be structured.

The real device structure of the thin film dielectric device **3** is not limited.

Examples of the device structure of the thin film dielectric device **3** are a planar type as shown in FIG. **1**, a stack type as shown in FIG. **2**, and a trench type as shown in FIG. **3**. In FIG. **3**, reference numeral **7** is an insulation layer for forming a trench. A trench **8** is formed on the insulation layer **7**. The present invention can be applied to a thin film capacitor that is a laminate film of the lower electrode **4**, the

dielectric thin film 5, and the upper electrode 6 that are disposed in the order.

As shown in FIGS. 4A and 4B, the laminate film portion of the lower electrode 4, the dielectric thin film 5, and the upper electrode 6 is a polycrystalline film having columnar grains A that succeed in the near vertical direction to the surface of the substrate. In other words, the lower electrode 4 is composed of a polycrystalline film having crystal grains (columnar grains) a that grow in the nearly vertical direction to the surface of the substrate. The dielectric thin film 5 successively grows from the crystal grains (columnar grains) a of the lower electrode 4. In addition, the dielectric thin film 5 has crystal grains (columnar grains) b that takes over the crystal orientation of the crystal grains a. The upper electrode 6 has crystal grains (columnar grains) c that successively grow from the crystal grains (columnar grains) b of the dielectric thin film 5 and take over the crystal orientation of the crystal grains b. FIG. 4A is a schematic diagram showing a fine structure of a laminate film of the lower electrode 4, the dielectric thin film 5, and the upper electrode 6. FIG. 4B is a photo taken by a microscope (TEM) showing a fine structure of a laminate film that has been actually fabricated.

The columnar grains A are composed of crystal grains a, b, and c that successively grow in the nearly vertical direction to the surface of the substrate. In the columnar grains A, the crystal grains b take over the size and crystal orientation of the crystal grains a of the dielectric thin film 5. In addition, the crystal grains c of the upper electrode 6 take over the size and crystal orientation of the crystal grains b of the dielectric thin film 5. In the columnar grains A, the lattice constants at individual interfaces are matched. The laminate film portion of the lower electrode 4, the dielectric thin film 5, and the upper electrode 6 is composed of a polycrystalline film of a group of the columnar grains A.

As described above, in the laminate film portion of the lower electrode 4, the dielectric thin film 5, and the upper electrode 6, with the columnar grains A, the lattice constant of the lower electrode 4 and the lattice constant of the dielectric thin film 5 are matched at the interface thereof. In addition, with the columnar grains A, the lattice constant of the dielectric thin film 5 and the lattice constant of the upper electrode 6 are matched at the interface thereof. In other words, the lattice constant of the lower electrode 4 and the lattice constant of the dielectric thin film 5 are matched at the interface thereof in the columnar grains A. In addition, the lattice constant of the dielectric thin film 5 and the lattice constant of the upper electrode 6 are matched in the columnar grains A. With the partial lattice-matching, a large amount of interface levels that suppresses an excessive leak current and a decrease of dielectric breakdown resistance is prevented from taking place. In other words, the thin film dielectric device 3 can remarkably suppress the increase of the leak current and the short-circuit. In addition, the thin film dielectric device 3 has an excellent dielectric breakdown resistance.

Moreover, since the laminate film portion of the lower electrode 4, the dielectric thin film 5, and the upper electrode 6 is basically the polycrystalline film having the columnar grains A, the laminate film portion can be properly formed on the plug 2 composed of poly-silicon (poly-Si) or tungsten (W). Thus, the thin film dielectric device 3 is not restricted by the substrate unlike with a conventional epitaxial growth film. Consequently, the thin film dielectric device 3 can be applied to a real LSI circuit having a semiconductor storing device such as a DRAM and an FRAM. The thin film dielectric device 3 according to the embodiment of the present invention can be applied to a real LSI circuit. In addition, the thin film dielectric device 3 suppresses an excessive leak current and the degradation of the dielectric breakdown resistance. The thin film dielectric device 3 has improved performance, reliability, and practicability.

When a polycrystalline film having columnar grains A whose size and crystal orientation succeed from the lower electrode 4 to the upper electrode 6 is fabricated, as the lower electrode 4 and the upper electrode 6, conductive materials whose lattice constants are similar to that of the dielectric thin film 5 are used. When each film is formed, the temperature of the substrate is raised. Alternatively, after each film is formed at a low temperature, the laminate film is heat-treated. Thus, a polycrystalline film having columnar grains A is obtained.

Each film can be formed by a variety of vapor growth method such as spatter method, vacuum evaporation method, and laser ablation method. When the polycrystalline film has the columnar grains A, it is preferred that the temperature of the substrate in the film forming stage is relatively high. The temperature of the substrate is preferably 673 K or more, more preferably, 873 K or more. When each film is formed at high temperature, the columnar grains A can be reproducibly obtained. Even if each film is formed at low temperature and then heat-treated, columnar grains A may be obtained. In this case, however, the lattice matching characteristic at the interface is lower than that of the high-temperature film forming method.

In addition, to improve the flatness of the surface of each interface, the lower electrode 4 is preferably formed in two stages. When the lower electrode 4 is formed by the spatter method, an initial film is formed with a low output.

Next, the lower electrode 4 is formed on the initial film for a predetermined thickness with a normal output. Since the initial film is formed with the lower output, the surface flatness of the lower electrode 4 can be improved. As with the lower electrode 4, the dielectric thin film 5 is preferably formed in two stages. The initial film is not limited to such a positively formed film, but a film of which atoms of a target in a cleaning stage are deposited.

In the relation between the grain size and electric characteristics of the dielectric thin film 5, the dielectric constant is proportional to the grain size. Since the grain size of the dielectric thin film 5 takes over the grain size of the lower electrode 4, the grain size of the lower electrode 4 is preferably large. From the view point of the grain size, each film is preferably formed in one stage. However, when each film is formed in one stage, the morphology at the interface may degrade. When each film is formed in two stages, by adjusting the temperature of the substrate in the film forming stage, the grain size can be controlled.

The size of the columnar grains A is preferably in the range from 5 to 500 nm. Each film should be formed so that the grain size is satisfied. When the size of the columnar grains A is less than 2 nm or larger than 1000 nm, it is difficult to successively grow the columnar grains from the lower electrode 4 to the upper electrode 6.

Next, the materials of the lower electrode 4 and the upper electrode 6 will be described. The mismatch of the lattice constant of the dielectric thin film 5 to the lattice constant of the lower portion 4 is preferably 15% or less. Thus, the material of the lower electrode 4 is selected so that the mismatch of the lattice constant is 15% or less. This condition applies to the upper electrode 6. When the mismatch of the lattice constant exceeds 15%, it is difficult to form the columnar grains A that succeed from the lower electrode 4 to the upper electrode 6.

As the materials of the lower electrode **4** and the upper electrode **6**, a conductive perovskite oxide with a thickness of 5 to 100 nm is preferably used so that the mismatch of the lattice constant to the dielectric thin film **5** composed of a perovskite oxide is 15% or less. As a conductive perovskite oxide, a variety of perovskite oxides having metal conductivity can be used.

Examples of the typical conductive perovskite oxide are $ARuO_3$ (where A is at least one element selected from the group consisting of Sr, Ba, Ca, La, and Nd) such as $SrRuO_3$ and $Sr_{1-x}Ba_xRuO_3$ ($0<x<1$) and $Sr_{1-x}RE_xCoO_3$ (where RE is at least one element selected from the group consisting of La, Pr, Sm, and Nd; $0 \leqq X \leqq 1$). These conductive perovskite oxides have excellent lattice matching characteristic to the perovskite oxide used for the dielectric thin film **5**.

The mismatch of the lattice constants of the electrodes **4** and **6** to lattice constant of the dielectric thin film **5** is preferably 5% or less. The lower the mismatch of the lattice constant, the higher the matching characteristic of the interface. In addition, the crystalline characteristics of the dielectric thin film **5** improves. As a result, a larger dielectric constant can be obtained. The mismatch of the lattice constants of the electrodes **4** and **6** to the lattice constant of the dielectric thin film **5** is more preferably 2.5% or less.

The lattice constants of the electrodes **4** and **6** and the dielectric thin film **5** can be varied by adjusting the composition of the perovskite oxide thereof. For example, at least one of the electrodes **4** and **6** and the dielectric thin film **5** is composed of a perovskite oxide of which A site is a perovskite oxide composed of at least two elements. In such a perovskite oxide, the lattice constant can be controlled by adjusting the composition of the A site elements. When for example Sn or Zn is added to the perovskite oxide, a B site element of the perovskite oxide may be substituted with such an element. With such an adjustment of the composition, the lattice constant can be controlled. The A site elements of the present invention represent elements that are placed in the A site of the perovskite structure that is basically expressed by ABO_3.

The lower electrode **4** may be composed of a layered perovskite oxide that has a conductive characteristic instead of a perovskite oxide expressed by ABO_3. The layered perovskite oxide contributes to improving the surface flatness of the lower electrode **4**. The layered perovskite oxide can be used for at least part of the lower electrode **4**.

The growth speed of the layered perovskite oxide largely varies in the crystal orientation. In the initial growth stage, the growth speed in the directions of axes a and b is higher than the growth speed in the direction of axis c. When a polycrystalline film of such a material is formed, the orientations of grains deposited in an island shape are at random in the initial film forming stage. However, as the film grows, the growth speed of grains in the surface direction (namely, axes a and b) becomes higher than the growth speed in the film thickness. Thus, in the film forming stage, grains are highly oriented in the direction of the film thickness (namely, axis c). Thereafter, since the growth speed in the direction of the film thickness of each grain is the same, a conductive perovskite oxide layer with an excellent crystalline characteristic and an excellent surface flatness can be obtained.

The layered perovskite oxide that is used for at least part of the lower electrode **4** and that has conductive characteristic is composed of a polycrystalline film of which grains are highly oriented on axis c in the direction of the film thickness (namely, polycrystalline film highly oriented on axis c). When the layered perovskite oxide that has conductive characteristic is formed on a base layer such as a plug **2**, a barrier layer, or an adhesion layer, the layered perovskite oxide becomes a polycrystalline film highly oriented on axis c. The polycrystalline film highly oriented on axis c has an excellent surface flatness.

Thus, when the dielectric thin film **5** composed of a perovskite oxide is formed on the lower electrode **4** composed of a layered perovskite oxide having conductive characteristic, since the dielectric thin film **5** grows taking over the surface flatness of the lower electrode **4**, the morphology at the interface of the lower electrode **4** and the dielectric thin film **5** can be improved. In addition, since the front surface of the dielectric thin film **5** has excellent surface flatness, the morphology at the interface of the dielectric thin film **5** and the upper electrode **6** is also excellent.

The layered perovskite oxide used for the lower electrode **4** preferably contain at least one transition metal element selected from the group consisting of Ru, Ir, Rh, Cr, Mn, Ni, and Co that have conductive characteristic. Particularly, in consideration of the application to the silicon process of an LSI circuit or the like, a layered perovskite oxide containing at least one transition metal element selected from the group consisting of Ru, Ir, and Rh is preferably used.

For example, such a layered perovskite oxide has a composition substantially expressed by the following formula.

General Formula:

$$AE_{n+1}TM_nO_{3n+1} \quad (1)$$

(where AE is at least one element selected from the group consisting of Sr, Ba, and Ca; TM is at least one transition metal element selected from Ru, Ir, and Rh; n is 1, 2, or 3).

In addition, considering the matching characteristic with BSTO or the like that is used for a dielectric, a layered perovskite oxide that is substantially expressed by the following formula.

General Formula:

$$Sr_{n+1}TM_nO_{3n+1} \quad (2)$$

(where TM is at least one transition element selected from the group consisting of Ru, Ir, and Rh; n is 1, 2, or 3).

In these layered perovskite oxides, as the value n increases, low dimensional characteristics of crystal structure and physical properties decrease. Thus, characteristics that are close to non-layered perovskite oxide (such as $AETMO_3$) are obtained. Thus, the value n is preferably 1, 2, or 3. When the value n is 4 or more, the surface flatness of the polycrystalline based on the orientation characteristic of the layered perovskite oxide may not be obtained.

Among the layered perovskite oxides expressed by Formula (2), at least one selected from the group consisting of Sr_2RuO_4, $Sr_3Ru_2O_7$, and $Sr_4Ru_3O_{10}$ is preferably used because of excellent stability and excellent conductive characteristic in wide film forming conditions.

In the layered perovskite oxides expressed by Formula (2), part of Sr is substituted with such as Ba or Ca so as to adjust the surface lattice constant (axes a and b) and thereby improving the lattice matching characteristic with BSTO or the like. In addition, part of alkali earth group metal element may be substituted with a rare earth element such as La or Nd.

The layered perovskite oxides having conductive characteristic are not limited to those expressed by Formulas (1)

and (2). For example, a layered perovskite oxide that has a composition substantially expressed by the following formula may be used.

General Formula:

$$A_{n+1}TM'_nO_{3n+1} \quad (3)$$

(where A is at least one element selected from the group consisting of a rare earth element and an alkali earth element; TM' is at least one transition metal element selected from the group consisting of Cr, Mn, Ni, and Co; n is 1, 2, or 3).

Examples of the layered perovskite oxides expressed by Formula (3) are $(La_{1-x}Sr_x)_2CoO_4$, $(La_{1-x}Sr_x)_3Co_2O_7$, $(La_{1-x}Sr_x)_4Co_3O_{10}$, $(La_{1-x}Sr_x)_2CrO_4$, $(La_{1-x}Sr_x)_3Mn_2O_7$, and $(La_{1-x}Sr_x)_3Ni_2O_7$.

In the layered perovskite oxide, as the value n increases, the low dimensional characteristics of crystal structure and physical properties decrease. Thus, the layered perovskite oxide has characteristics close to those of a non-layered perovskite oxide. Consequently, the conductivity in the direction of the film thickness increases. With this property, a laminate film of n layered perovskite oxides or a laminate film of a layered perovskite oxide and a non-layered perovskite oxide may be used for the lower electrode **4**.

FIG. **5** shows the structure of the lower electrode **4** composed of a laminate film of a first lower electrode layer **4***a* and a second lower electrode layer **4***b*. The first lower electrode layer **4***a* is composed of a polycrystalline film of a layered perovskite oxide expressed by Formula (1) or (2). The second lower electrode layer **4***b* is composed of a non-layered perovskite oxide such as $SrRuO_3$ and a layered perovskite oxide whose value n is large (for example, n=3, 4, . . .).

In other words, in an initial stage of which a film is formed immediately on the plug **2** or an intermediate layer, a layered perovskite oxide expressed by Formula (1) or (2), in particular, a layered perovskite oxide whose value n is 1 or 2 (highly oriented on axis c), is deposited until a successive film is obtained. Thus, the first lower electrode layer **4***a* composed of the polycrystalline film highly oriented on axis c is formed. The second lower electrode layer **4***b* composed of the non-layered perovskite oxide of which the conductivity in the direction of axis c is high is formed on the first lower electrode layer **4***a*.

In such a laminate film structure, the second lower electrode layer **4***b* takes over the crystal orientation of the first lower electrode layer **4***a*. The second lower electrode layer **4***b* becomes a highly oriented polycrystalline film. Thus, the conductivity in the direction of the film thickness of the lower electrode **4** is improved. In addition, the morphology at the interface with the dielectric thin film **5** can be suppressed from degrading.

FIG. **6** shows the structure of a lower electrode **4** composed of a first lower electrode layer **4***a*, a second lower electrode layer **4***b*, and a third lower electrode layer **4***c* disposed therebetween. The first lower electrode layer **4***a* is composed of a polycrystalline film of a layered perovskite oxide highly oriented on axis c. The second lower electrode layer **4***b* is composed of a non-layered perovskite oxide. The third lower electrode **4***c* is composed of a layered perovskite oxide whose value n is large (for example, n=3, 4, . . .).

The lower electrode **4** may be composed of a laminate film having different AE components (or A component), a laminate film having different TM components (or TM' components), or a laminate film of the combination thereof. Such a laminate film is effective for adjusting the lattice constant. Thus, with such a laminate film, the lower electrode **4** can be epitaxially grown at a local region. In addition, with such a laminate film, the surface flatness can be improved.

In the above-described embodiment, the columnar grains A are successively grown from the lower electrode **4** to the upper electrode **6**. However, the present invention is not limited to such a structure. Instead, one of the laminate film of the lower electrode **4** and the dielectric thin film **5** and the laminate film of the dielectric thin film **5** and the upper electrode **6** may be a polycrystalline film having the columnar grains A that succeed in the nearly vertical direction to the surface of the substrate. For example, the laminate film of the lower electrode **4** and the dielectric thin film **5** can be a polycrystalline film having the columnar grains A. The upper electrode **6** may be a Pt electrode.

When a noble metal such as Pt, Rh, Ru, Pd, Os, or Ir is used for the lower electrode **4** and the upper electrode **6**, the lattice constants of these noble metals are close to the lattice constant of the perovskite oxide, corresponding to the film forming conditions, the columnar grains A that succeed form the lower electrode **4** to the upper electrode **6** can be obtained.

Next, with reference to FIG. **7**, a thin film dielectric device according to another embodiment of the present invention will be described.

As with the above-described embodiment, a thin film dielectric device **9** shown in FIG. **7** is a polycrystalline film having columnar grains of which a laminate portion of a lower electrode **10**, a dielectric thin film **11**, and an upper electrode **12** succeed in the nearly vertical direction to the surface of a substrate. The lattice constants of these layers are matched at the interface thereof. At least one of the lower electrode **10** and the upper electrode **12** (for example, the lower electrode **10**) is composed of a conductive perovskite oxide whose lattice constant is smaller than the perovskite oxide that composes the dielectric thin film **11**. Thus, the dielectric thin film **11** has distortion induced ferroelectricity.

By adjusting the lattice constants of the lower electrode **10**, the upper electrode **12**, and the dielectric thin film **11**, a thin film dielectric device **9** that has distortion induced ferroelectricity can be fabricated. At this point, the conductive perovskite oxide of the lower electrode **10** and the upper electrode **12** and the perovskite oxide of the dielectric thin film **11** preferably satisfy the following conditions. In other words, assuming that the lattice constant of the perovskite oxide (dielectric) represented by the length of axis a of the perovskite crystal structure is denoted by ad and the lattice constant of the conductive perovskite oxide (electrode) represented by the length of axis a of the perovskite crystal structure is denoted by as, the relation of $1.002 \leqq ad/as \leqq 1.015$ should be satisfied. When the lattice constant ratio ad/as exceeds the above range, the distortion induced ferroelectricity may not take place.

A practical example of the material of the dielectric thin film **11** is $Ba_{1-x}Sr_xTiO_3$ (where $x \leqq 0.6$). Examples of the material of the lower electrode **10** and the upper electrode **12** are $AERuO_3$ (where AE is at least one element selected from the group consisting of Ba and Ca) and $Sr_{1-x}RE_xCoO_3$ (where RE is at least one element selected from the group consisting of La, Pr, Sm, and Nd; $0 \leqq x < 1$). At this point, part of AE of $AERuO_3$ may be substituted with for example La or Nd. With AE that is a mixture of Ca and Ba, the lattice constant can be controlled. When the lattice constant of the electrode is rather small, $Ba_{1-x}Sr_xTiO_3$ (where $X > 0.6$) can be used as the material of the dielectric thin film, and $SrTiO_3$ also has distortion induced ferroelectricity.

The polycrystalline film highly oriented on axis c of the layered perovskite oxide having conductive characteristic

can be effectively used for the lower electrode **10** and the upper electrode **12** of the thin film dielectric device **9** having the distortion induced ferroelectricity. An example of the material of the dielectric thin film **11** is $Ba_{1-x}Sr_xTiO_3$ (where $x \leqq 0.6$). Examples of the material of the lower electrode **10** are $(Sr_{1-y}Ba_y)_2RuO_4$, $(Sr_{1-y}Ba_y)_3Ru_2O_7$, and $(Sr_{1-y}Ba_y)_4Ru_3O_{10}$ ($0 \leqq y \leqq 0.5$).

The thin film dielectric device according to the present invention is not limited to semiconductor devices such as a DRAM and an FRAM. Instead, the thin film dielectric device may be formed on a GaAs substrate and used for a capacitor for a microwave. Alternatively, the thin film dielectric device can be used for thin film capacitors of various devices such as a lower power liquid crystal display unit that uses ferroelectricity.

Next, practical embodiments of the present invention and evaluation results thereof will be described.

First Embodiment

As shown in FIG. **1**, a $SrRuO_3$ film as a lower electrode **4** was deposited for 30 nm on an Si substrate **1** having a plug **2** composed of poly-silicon by RF magnetron spatter method. At this point, the temperature of the substrate was 873 K. Before the SrRuO3 film was formed, the shutter was closed and the target was cleaned. At this point, part of spatter atoms leaked from the shutter. Thus, an initial film of $SrRuO_3$ was deposited.

After the $SrRuO_3$ film was formed, a $Ba_{0.5}Sr_{0.5}TiO_3$ film as a dielectric thin film **5** was deposited for 20 nm on the lower electrode **4**. A $SrRuO_3$ film as an upper electrode **6** was deposited for 30 nm on the dielectric thin film **5**. Thus, a thin film capacitor for a DRAM was fabricated.

The section of the resultant thin film capacitor was observed by an electron microscope (TEM). As a result, the laminate film of the lower electrode **4**, the dielectric thin film **5**, and the upper electrode **6** is a polycrystalline film. The polycrystalline film was having columnar grains A of which the sizes of the dielectric thin film **5** and the upper electrodes **6** were the same in the direction of the substrate surface corresponding to the size of the crystal grains of the lower electrode **4** and the crystal orientations thereof were the same. The size in the direction of the surface of the columnar grains A was around 20 nm. In the columnar grains A, the lattice constant of the lower electrode **4** and the lattice constant of the dielectric thin film **5** were matched at the interface thereof. In addition, the lattice constant of the dielectric thin film **5** and the lattice constant of the upper electrode **6** were matched at the interface thereof. It was occasionally difficult to distinguish the boundary between each layer. As a result, ion defects hardly took place.

When the electric characteristic of the thin film capacitor according to the first embodiment was measured, the dielectric constant was 500 and the leak current at 1.8 V was 1×10^{-8} A/cm^2. When a voltage of DC 10 V was applied to the thin film capacitor, a dielectric breakdown did not take place.

When the thin film capacitor with the structure according to the first embodiment was formed on an Si substrate that does not have the plug **2**, the similar fine structure and characteristics were obtained.

Second Embodiment

As shown in FIG. **2**, a $SrRuO_3$ film was deposited for 30 nm on a Si substrate **1** having a plug **2** (formed by selective growth method) by RF magnetron spatter method (temperature of substrate=873 K). Before the $SrRuO_3$ film was formed, the cleaning step was performed as with the first embodiment. A lower electrode **4** with an area of 0.18 μm was etched out from the $SrRuO_3$ film by reactive ion etching (RIE) method. Thus, a stack type lower electrode was formed. A $Ba_{0.5}Sr_{0.5}TiO_3$ film for 20 nm as a dielectric thin film **5** and a $SrRuO_3$ film for 30 nm as an upper electrode **6** were formed on the lower electrode **4** by RF magnetron spatter method. Thus, a thin film capacitor for a DRAM was fabricated.

The section of the resultant thin film capacitor was observed by the electron microscope (TEM). As a result, the thin film capacitor had a columnar grain structure of which the interfaces of the lower electrode **4**, the dielectric thin film **5**, and the upper electrode **6** were matched on the side surface and the upper surface thereof. The size of the columnar grains in the direction of the surface thereof was around 30 nm. When the electric characteristics of the thin film capacitor according to the second embodiment were measured, the dielectric constant of the thin film capacitor was 500. The leak current at 1.8 V was 1×10^{-8} A/cm^2 or less. Even if a voltage of DC 10 V was applied to the thin film capacitor, a dielectric breakdown did not take place.

Third Embodiment

As shown in FIG. **3**, a SiO_2 insulation film **7** was formed for 300 nm on an Si substrate **1** having a plug **2** (formed by the selective growing method) by plasma TEOS method. A capacitor trench **8** was formed on the SiO_2 insulation layer **7** by lithograph process.

Next, a $SrRuO_3$ film for 30 nm as a lower electrode **4** was deposited on the SiO_2 insulation layer **7** including the capacitor trench **8** (temperature of substrate=873 K). Thereafter, the surface was flatted by CMP and cells were separated. Before the $SrRuO_3$ film was formed, the cleaning process as with the first embodiment was performed.

Thereafter, a $Ba_{0.5}Sr_{0.5}TiO_3$ film for 20 nm as a dielectric thin film **5** was formed on the lower electrode **4** by RF magnetron spatter method. A $SrRuO_3$ film for 30 nm as an upper electrode **6** was deposited on the dielectric thin film **5**. Thus, a thin film capacitor for a DRAM was fabricated.

The section of the resultant thin film capacitor was observed by the electron microscope (TEM). As a result, the laminate film of the lower electrode **4**, the dielectric thin film **5**, and the upper electrode **6** was a polycrystalline film. The polycrystalline film was having columnar grains of which the sizes of the dielectric thin film **5** and the upper electrodes **6** were the same in the direction of the substrate surface corresponding to the size of the crystal grains of the lower electrode **4** and the crystal orientations thereof were the same. The size in the direction of the surface of the columnar grains was around 30 nm. In the columnar grains, the lattice constant of the lower electrode **4** and the lattice constant of the dielectric thin film **5** were matched at the interface thereof. In addition, the lattice constant of the dielectric thin film **5** and the lattice constant of the upper electrode **6** were matched at the interface thereof. As a result, ion defects hardly took place.

When the electric characteristic of the thin film capacitor according to the third embodiment was measured, the dielectric constant was 500 and the leak current at 1.8 V was 1×10^{-8} A/cm^2. When a voltage of DC 10 V was applied to the thin film capacitor, a dielectric breakdown did not take place.

Fourth Embodiment

As with the third embodiment, a SiO_2 insulation film **7** was formed for 300 nm on an Si substrate **1** having a plug **2** by plasma TEOS method. A capacitor trench **8** was formed on the SiO_2 insulation layer **7** by lithograph process.

Next, a $La_{0.5}Sr_{0.5}CoO_3$ film for 30 nm as a lower electrode **4** was deposited on the SiO_2 insulation layer **7** including the capacitor trench **8** (temperature of substrate=873 K).

Thereafter, the surface was flatted by CMP and cells were separated. Before the $La_{0.5}Sr_{0.5}CoO_3$ film was formed, the cleaning process as with the first embodiment was performed.

Thereafter, a $Ba_{0.5}Sr_{0.5}TiO_3$ film for 20 nm as a dielectric thin film **5** was formed on the lower electrode **4** by RF magnetron spatter method. A $La_{0.5}Sr_{0.5}CoO_3$ film for 30 nm as an upper electrode **6** was deposited on the dielectric thin film **5**. Thus, a thin film capacitor for a DRAM was fabricated.

The section of the resultant thin film capacitor was observed by the electron microscope (TEM). As a result, the laminate film of the lower electrode **4**, the dielectric thin film **5**, and the upper electrode **6** was a polycrystalline film. The polycrystalline film was having columnar grains of which the sizes of the dielectric thin film **5** and the upper electrodes **6** were the same in the direction of the substrate surface corresponding to the size of the crystal grains of the lower electrode **4** and the crystal orientations thereof were the same. The size in the direction of the surface of the columnar grains was around 30 nm. In the columnar grains, the lattice constant of the lower electrode **4** and the lattice constant of the dielectric thin film **5** were matched at the interface thereof. In addition, the lattice constant of the dielectric thin film **5** and the lattice constant of the upper electrode **6** were matched at the interface thereof.

When the electric characteristic of the thin film capacitor according to the third embodiment was measured, the dielectric constant was 470 and the leak current at 1.8 V was 1×10^{-8} A/cm^2. When a voltage of DC 10 V was applied to the thin film capacitor, a dielectric breakdown did not take place.

Fifth Embodiment

A $Ba_{0.12}Sr_{0.88}TiO_3$ film for 20 nm as a dielectric thin film was formed on a $SrRuO_3$ film (lower electrode) formed in the same manner as the first embodiment. A $SrRuO_3$ film for 30 nm as an upper electrode was deposited on the dielectric thin film. Thus, a thin film capacitor for a DRAM was fabricated.

The section of the resultant thin film capacitor was observed by the electron microscope (TEM). As a result, the laminate film of the lower electrode, the dielectric thin film, and the upper electrode was having columnar grains of which the size of each layer in the direction of the surface of the substrate was the same and the crystal orientation of each layer was the same. When the X ray diffraction of the thin film capacitor was measured, the peaks of the $SrRuO_3$ film and the $Ba_{0.12}Sr_{0.88}TiO_3$ film overlapped. The estimated lattice constant was 0.398 nm.

The electric characteristics of the thin film capacitor according to the fifth embodiment were measured. The dielectric constant of the thin film capacitor was 550. The leak current of the thin film capacitor at 1.8 V was 1×10^{-8} A/cm^2 or less. When a voltage of DC 10 V was applied to the thin film capacitor, dielectric breakdown did not take place. The dielectric constant of the thin film capacitor according to the fifth embodiment was higher than the dielectric constant of the thin film capacitor according to the first embodiment. This is because the matching of the lattice constants accelerates crystal growth, thereby improving crystalline characteristics.

Sixth Embodiment

A $Ba_{0.12}Sr_{0.88}TiO_3$ film for 20 nm as a dielectric thin film was formed on a $SrRuO_3$ film (lower electrode) formed in the same manner as the second embodiment. A $SrRuO_3$ film for 30 nm as an upper electrode was deposited on the dielectric thin film. Thus, a thin film capacitor for a DRAM was fabricated.

The section of the resultant thin film capacitor was observed by the electron microscope (TEM). As a result, the laminate film of the lower electrode, the dielectric thin film, and the upper electrode was having columnar grains of which the size of each layer in the direction of the surface of the substrate was the same and the crystal orientation of each layer was the same. When the X ray diffraction of the thin film capacitor was measured, the peaks of the $SrRuO_3$ film and the $Ba_{0.12}Sr_{0.88}TiO_3$ film overlapped. The estimated lattice constant was 0.398 nm.

The electric characteristics of the thin film capacitor according to the sixth embodiment were measured. The dielectric constant of the thin film capacitor was 550. The leak current of the thin film capacitor at 1.8 V was 1×10^{-8} A/cm^2 or less. When a voltage of DC 10 V was applied to the thin film capacitor, dielectric breakdown did not take place.

Seventh Embodiment

A $Ba_{0.12}Sr_{0.88}TiO_3$ film for 20 nm as a dielectric thin film was formed on a $SrRuO_3$ film (lower electrode) formed in the same manner as the third embodiment. A $SrRuO_3$ film for 30 nm as an upper electrode was deposited on the dielectric thin film. Thus, a thin film capacitor for a DRAM was fabricated.

The section of the resultant thin film capacitor was observed by the electron microscope (TEM). As a result, the laminate film of the lower electrode, the dielectric thin film, and the upper electrode was having columnar grains of which the size of each layer in the direction of the surface of the substrate was the same and the crystal orientation of each layer was the same. When the X ray diffraction of the thin film capacitor was measured, the peaks of the $SrRuO_3$ film and the $Ba_{0.12}Sr_{0.88}TiO_3$ film overlapped. The estimated lattice constant was 0.398 nm.

The electric characteristics of the thin film capacitor according to the seventh embodiment were measured. The dielectric constant of the thin film capacitor was 550. The leak current of the thin film capacitor at 1.8 V was 1×10^{-8} A/cm^2 or less. When a voltage of DC 10 V was applied to the thin film capacitor, dielectric breakdown did not take place.

Eighth Embodiment

A $Ba_{0.12}Sr_{0.88}TiO_3$ film for 20 nm as a dielectric thin film was formed on a $La_{0.1}Sr_{0.9}CoO_3$ film (lower electrode) formed in the same manner as the fourth embodiment. A $La_{0.1}Sr_{0.9}CoO_3$ film for 30 nm as an upper electrode was deposited on the dielectric thin film. Thus, a thin film capacitor for a DRAM was fabricated.

The section of the resultant thin film capacitor was observed by the electron microscope (TEM). As a result, the laminate film of the lower electrode, the dielectric thin film, and the upper electrode was having columnar grains of which the size of each layer in the direction of the surface of the substrate was the same and the crystal orientation of each layer was the same. When the X ray diffraction of the thin film capacitor was measured, the peaks of the $La_{0.1}Sr_{0.9}CoO_3$ film and the $Ba_{0.1}Sr_{0.9}TiO_3$ film overlapped. The estimated lattice constant was 0.398 nm.

The electric characteristics of the thin film capacitor according to the eighth embodiment were measured. The dielectric constant of the thin film capacitor was 520. The leak current of the thin film capacitor at 1.8 V was 1×10^{-8} A/cm^2 or less. When a voltage of DC 10 V was applied to the thin film capacitor, dielectric breakdown did not take place.

Ninth Embodiment

A reverse spatter process was performed so as to clean the surface of the substrate in an Ar (=50 sccm) atmosphere for five minutes with an RF output of 120 W.

A $SrRuO_3$ film as a lower electrode was formed on the substrate by the spatter process in an Ar/O_2 (=40/10 sccm) atmosphere. The pressure in the chamber in the spatter stage was 0.7 Pa. The distance between the target and the substrate was 85 mm. The $SrRuO_3$ film was formed in two stages. As the film forming conditions in the first stage, the RF output was 90 W and the spatter time was 10 min. As the film forming conditions in the second stage, the RF output was 300 W and the spatter time was 20 min. The temperature of the substrate was 873 K. The thickness of the $SrRuO_3$ film was around 30 nm.

Next, a $Ba_{0.5}Sr_{0.5}TiO_3$ film as a dielectric film was formed on the $SrRuO_3$ film in an Ar/O_2 (=40/10 sccm) atmosphere by the spatter method. The pressure in the chamber in the spatter stage was 0.7 Pa. The distance between the target and the substrate was 140 mm. The $Ba_{0.5}Sr_{0.5}TiO_3$ film was formed in two stages. As film forming conditions in the first stage, the RF output was 60 W and the spatter time was 10 min. As film forming conditions in the second stage, the RF output was 500 W and the spatter time was 10 min. The temperature of the substrate was 873 K. The thickness of the $Ba_{0.5}Sr_{0.5}TiO_3$ film was around 20 nm.

A $SrRuO_3$ film as an upper electrode was formed on the $Ba_{0.5}Sr_{0.5}TiO_3$ film in the same conditions as the lower electrode. Thus, a thin film capacitor for a DRAM was fabricated.

On the other hand, a thin film capacitor for a DRAM was fabricated in the same conditions except that each film was formed in one stage. The film forming conditions of each film were the same as those of the second stage.

The section of each thin film capacitor was observed by the electron microscope (TEM). As a result, the laminate film of the lower electrode **4**, the dielectric thin film **5**, and the upper electrode **6** was having columnar grains of which the size of each layer in the direction of the surface of the substrate was the same and the crystal orientation of each layer was the same. When each film was formed in two stages, the size of the columnar grains in the direction of the surface was around 75 nm. When each film was formed in one stage, the size of the columnar grains in the direction of the surface was around 113 nm.

The electric characteristics of each thin film capacitor were measured. The dielectric constant was measured by an LCR meter in conditions that the measured frequency was 100 k and the amplitude was 0.1 V. The dielectric constant of the thin film capacitor formed in two stages was around 520. The dielectric constant of the thin film capacitor formed in one stage was around 570. The leak current of the thin film capacitor formed in two stages was 1×10^{-8} A/cm^2 at ±3 V. The leak current of the thin film capacitor formed in one stage was 1×10^{-8} A/cm^2 at 1 V. This situation results from a protrusion due to an abnormal grain growth.

Tenth to Nineteenth Embodiments

As shown in FIG. **3**, a SiO_2 insulation layer **7** was formed for 100 nm on an Si substrate **1** having a plug **2** (composed of poly-silicon) by plasma TEOS method. A capacitor trench **8** was formed on a SiO_2 insulation layer **7** by lithography process. A TiAlN film for 10 nm and a Pt film for 10 nm were successively deposited as intermediate layers on the insulation layer **7** including the capacitor trench **8** by DC spatter method.

Next, a lower electrode **4** was deposited by RF magnetron spatter method. Thereafter, the front surface was flattened by CMP method. In addition, cells were separated. A dielectric thin film **5** was deposited on the lower electrode **4** by the RF magnetron spatter method. An upper electrode **6** was deposited on the dielectric thin film **5**. Table 1 shows the structural material and film thickness of the lower electrode **4**, the dielectric thin film **5**, and the upper electrode **6** of each of the thin film capacitors for DRAMs according to tenth embodiment to nineteenth embodiment.

Samples for a transmission electron microscope were made from the thin film capacitors according to the tenth embodiment to the nineteenth embodiment. The samples were observed by the transmission type electron microscope. As a result, the lower electrode was a polycrystalline film highly oriented on axis c. In addition, the dielectric thin film and the upper electrode were highly oriented films that had an interface of a local epitaxial structure that took over the crystal orientation. The morphology at the interface of the lower electrode and the dielectric thin film and at the interface of the dielectric thin film and the upper electrode were excellent. The average roughness was 1 nm or less.

The electric characteristics of the thin film capacitors according to the individual embodiments were measured. Table 1 shows the dielectric constant of each thin film capacitor. The leak current density at 2.5 V was 1×10^{-8} A/cm^2 or less. When a voltage of DC 10 V was applied, dielectric breakdown did not take place.

TABLE 1

	Lower electrode	Dielectric thin film	Upper electrode	Electric constant
Tenth embodiment	Sr2RuO4 (30 nm)	Ba0.2Sr0.8 TiO3 (20 nm)	Sr2RuO4 (100 nm)	490
Eleventh embodiment	Sr3Ru2O7 (30 nm)	Ba0.2Sr0.8 TiO3 (20 nm)	Sr3Ru2O7 (100 nm)	480
Twelfth embodiment	Sr4Ru3O10 (30 nm)	Ba0.2Sr0.8 TiO3 (20 nm)	Sr4Ru3O10 (30 nm)	500
Thirteenth embodiment	Sr2IrO4 (30 nm)	Ba0.2Sr0.8 TiO3 (20 nm)	Sr2IrO4 (100 nm)	490
Fourteenth embodiment	Sr3Ir2O7 (30 nm)	Ba0.2Sr0.8 TiO3 (20 mn)	Sr3Ir2O7 (100 nm)	480
Fifteenth embodiment	Sr4Ir3O10 (30 nm)	Ba0.2Sr0.8 TiO3 (20 nm)	Sr4Ir3O10 (30 nm)	500
Sixteenth embodiment	Sr2RhO4 (30 nm)	Ba0.2Sr0.8 TiO3 (20 nm)	Sr2RhO4 (100 nm)	490
Seventeenth embodiment	Sr3Rh2O7 (30 nm)	Ba0.2Sr0.8 TiO3 (20 nm)	Sr3Rh2O7 (100 nm)	480
Eighteenth embodiment	Sr4Rh3O10 (30 nm)	Ba0.2Sr0.8 TiO3 (20 nm)	Sr4Rh3O10 (30 nm)	500
Nineteenth embodiment	Sr2RuO4 (10 nm)/ SrRuO3 (20 nm)	Ba0.2Sr0.8 TiO3 (20 nm)	SrRuO3 (100 nm)	480

Twentieth Embodiment

As shown in FIG. **5**, a $SrRuO_3$ film as a lower electrode **10** was deposited for 30 nm on a Si substrate having a plug **2** composed of poly-silicon by RF magnetron spatter method. At this point, the temperature of the substrate was 873 K. A $Ba_{0.8}Sr_{0.2}TiO_3$ film as a dielectric thin film **11** was deposited for 20 nm on the lower electrode **10**. A $SrRuO_3$ film as an upper electrode **13** was deposited for 30 nm on the dielectric thin film **11**. Thus, a thin film capacitor for an FRAM was fabricated.

The section of the resultant thin film capacitor was observed by the electron microscope (TEM). As a result, the laminate film of the lower electrode **10**, the dielectric thin

film **11**, and the upper electrode **12** was a polycrystalline film. The polycrystalline film was having columnar grains of which the sizes of the dielectric thin film **11** and the upper electrodes **12** were the same in the direction of the substrate surface corresponding to the size of the crystal grains of the lower electrode **10** and the crystal orientations thereof were the same. In the columnar grains, the lattice constant of the lower electrode **10** and the lattice constant of the dielectric thin film **11** were matched at the interface thereof. In addition, the lattice constant of the dielectric thin film **11** and the lattice constant of the upper electrode **12** were matched at the interface thereof. It was occasionally difficult to distinguish the boundary between each layer. As a result, ion defects hardly took place.

When the X-ray diffraction of the fabricated sample was measured, the lattice constant of axis c of the $SrRuO_3$ film as the lower electrode **10** and the upper electrode **12** was 0.398 nm. The lattice constant of axis c of the $Ba_{0.8}Sr_{0.2}TiO_3$ film as the dielectric thin film **11** was 0.403 nm. FIG. **8** shows a hysteresis curve of polarization to electric field (P-E) of the fabricated thin film capacitor. In this embodiment, with a soyatower circuit, an AC voltage at 5 kHz was applied and a hysteresis curve was measured at a room temperature. As is clear from FIG. **8**, the polarization of the thin film capacitor represents a hysteresis due to the relation with the applied electric field.

In the thin film capacitor according to this embodiment, the $Ba_{0.8}Sr_{0.2}TiO_3$ thin film had ferroelectricity. The intensity of the residual dielectric obtained from the hysteresis curve shown in FIG. **8** was as large as 0.11 C/m^2. When the electric characteristics of the thin film capacitor according to the embodiment were measured, the dielectric constant thereof was 600 and the leak current at 1.8 V was 1×10^{-8} A/cm^2 or less. When a voltage of DC 10 V was applied to the thin film capacitor, dielectric breakdown did not take place. Thus, the thin film capacitor according to this embodiment can be used for an FRAM.

Twenty-First Embodiment

As with the twentieth embodiment, a $La_{0.5}Sr_{0.5}CoO_3$ film as a lower electrode **10** was deposited for 300 nm on a Si substrate having a plug **2** composed of poly-silicon by RF magnetron spatter method. At this point, the temperature of the substrate was 873 K. A $Ba_{0.8}Sr_{0.2}TiO_3$ film as a dielectric thin film **11** was deposited for 20 nm on the lower electrode **10**. A $La_{0.5}Sr_{0.5}CoO_3$ film as an upper electrode **12** was deposited for 30 nm on the dielectric thin film **11**. Thus, a thin film capacitor for an FRAM was fabricated.

The section of the resultant thin film capacitor was observed by the electron microscope (TEM). As a result, the laminate film of the lower electrode **10**, the dielectric thin film **11**, and the upper electrode **12** was a polycrystalline film. The polycrystalline film was having columnar grains of which the sizes of the dielectric thin film **11** and the upper electrodes **12** were the same in the direction of the substrate surface corresponding to the size of the crystal grains of the lower electrode **10** and the crystal orientations thereof were the same. In the columnar grains, the lattice constant of the lower electrode **10** and the lattice constant of the dielectric thin film **11** were matched at the interface thereof. In addition, the lattice constant of the dielectric thin film **11** and the lattice constant of the upper electrode **12** were matched at the interface thereof. It was occasionally difficult to distinguish the boundary between each layer. As a result, ion loss hardly took place.

When the X-ray diffraction of the fabricated sample was measured, the lattice constant of axis c of the $La_{0.5}Sr_{0.5}CoO_3$ film as the lower electrode **10** and the upper electrode **12** was 0.389 nm. The lattice constant of axis c of the $Ba_{0.8}Sr_{0.2}TiO_3$ film as the dielectric thin film **11** was 0.403 nm. As with the twentieth embodiment, the hysteresis curve of polarization to electric field (P-E) of the fabricated thin film capacitor was measured. As a result, a hysteresis curve as shown in FIG. **8** was obtained. As is clear from FIG. **8**, the polarization of the thin film capacitor represents a hysteresis due to the relation with the applied electric field.

In other words, in the thin film capacitor according to this embodiment, the $Ba_{0.8}Sr_{0.2}TiO_3$ thin film had ferroelectricity. The intensity of the residual dielectric obtained from the hysteresis curve was as large as 0.12 C/m^2. When the electric characteristics of the thin film capacitor according to the embodiment were measured, the dielectric constant thereof was 610 and the leak current at 1.8 V was 1×10^{-8} A/cm^2 or less. When a voltage of DC 10 V was applied to the thin film capacitor, dielectric breakdown did not take place. Thus, the thin film capacitor according to this embodiment can be used for an FRAM.

Twenty-Second Embodiment

As with the twentieth embodiment, a $Nd_{0.5}Sr_{0.5}CoO_3$ film as a lower electrode **10** was deposited for 300 nm on a Si substrate having a plug **2** composed of poly-silicon by RF magnetron spatter method. At this point, the temperature of the substrate was 873 K. A $Ba_{0.8}Sr_{0.2}TiO_3$ film as a dielectric thin film **11** was deposited for 20 nm on the lower electrode **10**. A $Nd_{0.5}Sr_{0.5}CoO_3$ film as an upper electrode **12** was deposited for 30 nm on the dielectric thin film **11**. Thus, a thin film capacitor for an FRAM was fabricated.

The section of the resultant thin film capacitor was observed by the electron microscope (TEM). As a result, the laminate film of the lower electrode **10**, the dielectric thin film **11**, and the upper electrode **12** was a polycrystalline film. The polycrystalline film was having columnar grains of which the sizes of the dielectric thin film **11** and the upper electrodes **12** were the same in the direction of the substrate surface corresponding to the size of the crystal grains of the lower electrode **10** and the crystal orientations thereof were the same. In the columnar grains, the lattice constant of the lower electrode **10** and the lattice constant of the dielectric thin film **11** were matched at the interface thereof. In addition, the lattice constant of the dielectric thin film **11** and the lattice constant of the upper electrode **12** were matched at the interface thereof. It was occasionally difficult to distinguish the boundary between each layer. As a result, ion loss hardly took place.

When the X-ray diffraction of the fabricated sample was measured, the lattice constant of axis c of the $Nd_{0.5}Sr_{0.5}CoO_3$ film as the lower electrode **10** and the upper electrode **12** was 0.386 nm. The lattice constant of axis c of the $Ba_{0.8}Sr_{0.2}TiO_3$ film as the dielectric thin film **11** was 0.403 nm. As with the twentieth embodiment, the hysteresis curve of polarization to electric field (P-E) of the fabricated thin film capacitor was measured. As a result, a hysteresis curve as shown in FIG. **8** was obtained. As is clear from FIG. **8**, the polarization of the thin film capacitor represents a hysteresis due to the relation with the applied electric field.

In other words, in the thin film capacitor according to this embodiment, the $Ba_{0.8}Sr_{0.2}TiO_3$ thin film had ferroelectricity. The intensity of the residual dielectric obtained from the hysteresis curve was as large as 0.10 C/m^2. When the electric characteristics of the thin film capacitor according to the embodiment were measured, the dielectric constant thereof was 580 and the leak current at 1.8 V was 1×10^{-8} A/cm^2 or less. When a voltage of DC 10 V was applied to the thin film capacitor, dielectric breakdown did not take place. Thus, the thin film capacitor according to this embodiment can be used for an FRAM.

In the thin film capacitors for the FRAMs according to the twentieth to twenty-second embodiments, as with the ninth embodiment, the two-stage film forming method can be used. With the two-stage film forming method, more excellent results can be obtained.

Twenty-Third to Thirty-Second Embodiments

As shown in FIG. **2**, a TiAlN film for 10 nm and a Pt film for 10 nm were formed as intermediate layers on a Si substrate **1** having a plug **2** composed of poly-silicon by DC spatter method.

Thereafter, a lower electrode **4** was deposited by RF magnetron spatter method. Cells were etched out and separated. A dielectric thin film **5** was deposited on the lower electrode **4** by the RF magnetron spatter method. An upper electrode **6** was deposited on the dielectric thin film **5**. Thus, a thin film capacitor for an FRAM was fabricated. Table 2 shows the material and film thickness of each of the lower electrode **4**, the dielectric thin film, and the upper electrode. Thus, the thin film capacitors for FRAMs according to the twenty-third to the thirty-second embodiments were fabricated.

Samples for a transmission electron microscope were made from the thin film capacitors according to the twenty-third embodiment to the thirty-second embodiment. The samples were observed by the transmission type electron microscope. As a result, the lower electrode was a polycrystalline film highly oriented on axis c. In addition, the dielectric thin film and the upper electrode were highly oriented films that had an interface of a local epitaxial structure that took over the crystal orientation.

The lattice constant of each dielectric thin film of each sample was measured. The lattice constant (the length of axis c) in the vertical direction to the surface of the substrate of the $Ba_{0.5}Sr_{0.5}TiO_3$ film was 0.410 nm that was much larger than the length of axis c of the conventional polycrystalline film (0.401 nm).

In addition, the electric characteristics of the thin film capacitors according to these embodiments were measured. As a result, the thin film capacitors have ferroelectricity. FIG. **2** shows the residual polarization and resistance against electric field of each embodiment.

TABLE 2

	Lower electrode	Ferroelectric thin film	Upper electrode	Residual polarization (C/m2)	Resistance against electric field
Twenty-third embodiment	Sr2RuO4 (30 nm)	Ba0.8Sr0.2 TiO3 (20 nm)	Sr2RuO4 (100 nm)	0.35	3.2
Twenty-fourth embodiment	Sr3Ru2O7 (30 nm)	Ba0.8Sr0.2 TiO3 (20 nm)	Sr3Ru2O7 (100 nm)	0.35	3.2
Twenty-fifth embodiment	Sr4Ru3O10 (30 nm)	Ba0.8Sr0.2 TiO3 (20 nm)	Sr4Ru3O10 (100 nm)	0.35	3.2
Twenty-sixth embodiment	Sr2IrO4 (30 nm)	Ba0.8Sr0.2 TiO3 (20 nm)	Sr2IrO4 (100 nm)	0.34	3.1
Twenty-seventh embodiment	Sr3Ir2O7 (30 nm)	Ba0.8Sr0.2 TiO3 (20 nm)	Sr3Ir2O7 (100 nm)	0.30	3.2
Twenty-eighth embodiment	Sr4Ir3O10 (30 nm)	Ba0.8Sr0.2 TiO3 (20 nm)	Sr4Ir3O10 (100 nm)	0.30	3.2
Twenty-ninth embodiment	Sr2RhO4 (30 nm)	Ba0.8Sr0.2 TiO3 (20 nm)	Sr2RhO4 (100 nm)	0.35	3.2
Thirtieth embodiment	Sr3Rh2O7 (30 nm)	Ba0.8Sr0.2 TiO3 (20 nm)	Sr3Rh2O7 (100 nm)	0.30	3.2
Thirty-first embodiment	Sr4Rh3O10 (30 nm)	Ba0.8Sr0.2 TiO3 (20 nm)	Sr4Rh3O10 (100 nm)	0.30	3.2
Thirty-second embodiment	Sr2RuO4 (10 nm)/ SrRuO3 (20 nm)	Ba0.8Sr0.2 TiO3 (20 nm)	SrRuO3 (100 nm)	0.35	3.2

Next, another embodiment will be described.

A layered perovskite oxide film composed of $Sr_{0.2}RuO_3$, $Sr_3Ru_2O_7$, $Sr_4Ru_3O_{10}$, or the like as a lower electrode was epitaxially grown on a $SrTiO_3$ substrate by RF magnetron spatter method. A $Ba_{0.2}Sr_{0.8}TiO_3$ film as a dielectric thin film was epitaxially grown on the lower electrode by the RF magnetron spatter method. A layered perovskite oxide film as an upper electrode was epitaxially grown on the dielectric thin film. Thus, a thin film capacitor for a DRAM was fabricated. When electric characteristics of the thin film capacitor were measured, an excellent dielectric constant was obtained. In addition, excellent results for leak current and dielectric breakdown resistance were obtained. A layered perovskite oxide is effective when each film composing a thin film capacitor is epitaxially grown.

Although the present invention has been shown and described with respect to best mode embodiments thereof, it should be understood by those skilled in the art that the foregoing and various other changes, omissions, and additions in the form and detail thereof may be made therein without departing from the spirit and scope of the present invention.

What is claimed is:

1. A thin film dielectric device, comprising:

a substrate having a capacitor surface;

a lower electrode formed on said substrate and composed of a polycrystalline film having columnar grains that have grown in a vertical to a capacitor surface of said substrate;

a dielectric thin film formed on said lower electrode and composed of a perovskite oxide, said dielectric thin film being a polycrystalline film having columnar grains that have successively grown from the columnar grains of said lower electrode and that takes over a crystal orientation of said lower electrode in each of said columnar grains of said dielectric thin film, the lattice constant of said dielectric thin film being in each of said columnar grains thereof substantially matched with the lattice constant of said lower electrode at the interface with the columnar grains of said lower electrode; and

an upper electrode formed on said dielectric thin film.

2. The thin film dielectric device as set forth in claim 1,

wherein said upper electrode is composed of a polycrystalline film having columnar grains that have successively grown from the columnar grain of said dielectric thin film and that has taken over a crystal orientation of said dielectric thin film in each of said columnar grains of said upper electrode, the lattice constant of said upper electrode being substantially matched in each of said columnar grains thereof with the lattice constant of said dielectric thin film at the interface with the columnar grains of said dielectric thin film.

3. The thin film dielectric device as set forth in claim 1,

wherein the mismatch of the lattice constant of said dielectric thin film to the lattice constant of said lower electrode is 15% or less.

4. The thin film dielectric device as set forth in claim 1,

wherein said lower electrode is composed of a conductive perovskite oxide.

5. The thin film dielectric device as set forth in claim 1,

wherein said lower electrode is at least one selected from the group consisting of $ARuO_3$ (where A is at least one element selected from the group consisting of Sr, Ba, Ca, La, and Nd) and $Sr_{1-x}RE_xCoO_3$ (where RE is at least one element selected from the group consisting of La, Pr, Sm, and Nd).

6. The thin film dielectric device as set forth in claim 4,

wherein the mismatch of the lattice constant of the perovskite oxide composing said dielectric thin film to the lattice constant of the conductive perovskite oxide composing said lower electrode is 15% or less.

7. The thin film dielectric device as set forth in claim 4,

wherein the mismatch of the lattice constant of the perovskite oxide composing said dielectric thin film to the lattice constant of the conductive perovskite oxide composing said lower electrode is 5% or less.

8. The thin film dielectric device as set forth in claim 7,

wherein at least one of the conductive perovskite oxide composing said lower electrode and the perovskite oxide composing said dielectric thin film is composed of a perovskite oxide having two or more A site elements, the two or more A site elements having a composition at which the mismatch of the lattice constant of said dielectric thin film to the lattice constant of said lower electrode being 5% or less.

9. The thin film dielectric device as set forth in claim 1,

wherein said substrate is composed of a semiconductor substrate.

10. The thin film dielectric device as set forth in claim 1,

wherein said lower electrode has at least a layered perovskite oxide layer.

11. The thin film dielectric device as set forth in claim 10,

wherein the layered perovskite oxide has at least one transition metal element selected from the group consisting of Ru, Ir, Rh, Cr, Mn, Ni, and Co.

12. The thin film dielectric device as set forth in claim 10,

wherein the layered perovskite oxide has a composition substantially expressed by the following formula

$$AE_{n+1}TM_nO_{3n+1}$$

(where AE is at least one element selected from the group consisting of Sr, Ba, and Ca; TM is at least one transition metal element selected from the group consisting of Ru, Ir, and Rh; and n is 1, 2, or 3).

13. The thin film dielectric device as set forth in claim 10,

wherein the layered perovskite oxide is composed of at least one selected from the group consisting of Sr_2RuO_4, $Sr_3Ru_2O_7$, and $Sr_4Ru_3O_{10}$.

14. The thin film dielectric device as set forth in claim 1,

wherein said lower electrode is composed of a conductive perovskite oxide having a lattice constant smaller than the lattice constant of said dielectric thin film so as to cause said dielectric thin film to have distortion induced ferroelectricity.

15. The thin film dielectric device as set forth in claim 14,

wherein assuming that the lattice constant of the perovskite oxide represented by the length of axis a of a perovskite crystal structure is denoted by ad and that the lattice constant of the conductive perovskite oxide represented by the length of axis a of the perovskite crystal structure is denoted by as, the relation of $1.002 \leqq ad/as \leqq 1.015$ is satisfied.

16. A thin film dielectric device, comprising:

a substrate having a capacitor surface;

a lower electrode formed on said substrate;

a dielectric thin film formed on said lower electrode and composed of a perovskite oxide, said dielectric thin film being a polycrystalline film having columnar grains that have grown in a vertical to the capacitor surface of said substrate; and

an upper electrode formed on said dielectric thin film, said upper electrode being composed of a polycrystalline film having columnar grains that have successively grown from the columnar grains of said dielectric thin film and that have taken over the crystal orientation of said dielectric thin film in each of said columnar grains of said upper electrode, the lattice constant of said upper electrode being in each of said columnar grains thereof substantially matched with the lattice constant of said dielectric thin film at the interface with the columnar grains of said dielectric thin film.

17. The thin film dielectric device as set forth in claim 16,

wherein the mismatch of the lattice constant of said dielectric thin film to the lattice constant of said upper electrode is 15% or less.

18. The thin film dielectric device as set forth in claim 16,

wherein said upper electrode is composed of a conductive perovskite oxide.

19. The thin film dielectric device as set forth in claim 16, wherein said upper electrode is at least one selected from the group consisting of $ARuO_3$ (where A is at least one element selected from the group consisting of Sr, Ba, Ca, La, and Nd) and $Sr_{1-x}RE_xCoO_3$ (where RE is at least one element selected from the group consisting of La, Pr, Sm, and Nd).

20. The thin film dielectric device as set forth in claim 18, wherein the mismatch of the lattice constant of the perovskite oxide composing said dielectric thin film to the lattice constant of the conductive perovskite oxide composing said upper electrode is 15% or less.

21. The thin film dielectric device as set forth in claim 18, wherein the mismatch of the lattice constant of the perovskite oxide composing said dielectric thin film to the lattice constant of the conductive perovskite oxide composing said upper electrode is 5% or less.

22. The thin film dielectric device as set forth in claim 21, wherein at least one of the perovskite oxide composing said dielectric thin film and the conductive perovskite oxide composing said upper thin film is composed of a perovskite oxide having two or more A site elements, the two or more A site elements having a composition at which the mismatch of the lattice constant of said dielectric thin film to the lattice constant of said upper electrode being 5% or less.

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